Development of track detection system in test beamlines using HL-LHC ATLAS silicon pixel detector

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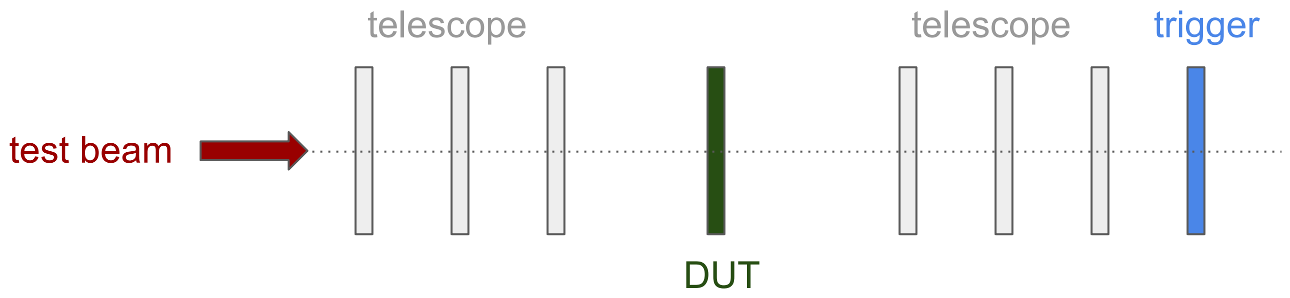
2022/12/22 Year-end presentation

Telescope

- Test beamlines
  - charged particle beam
  - test a detector (DUT = device under test)
- Telescope
  - reconstruct track -> reference



Resolution of telescope

❖ existence probability density :

$$P\left(x\right) = \frac{1}{d}$$

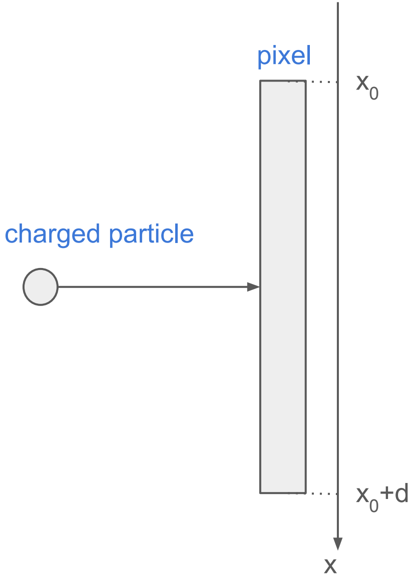
❖ expected value of incident position :

$$E(x) = \int_{x_0}^{x_0+d} P(x)x\,dx = x_0 + \frac{d}{2}$$

❖ resolution :

$$\sigma_x{}^2 = \int_{x_0}^{x_0+d} P\left(x\right)\times\left(x - E(x)\right)^2 dx \; = \frac{d^2}{12}$$

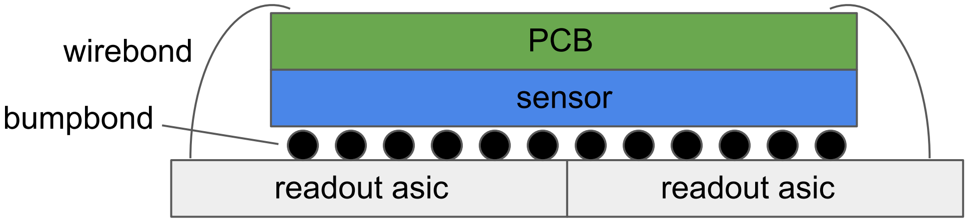
$$\sigma_x = \frac{d}{\sqrt{12}}$$

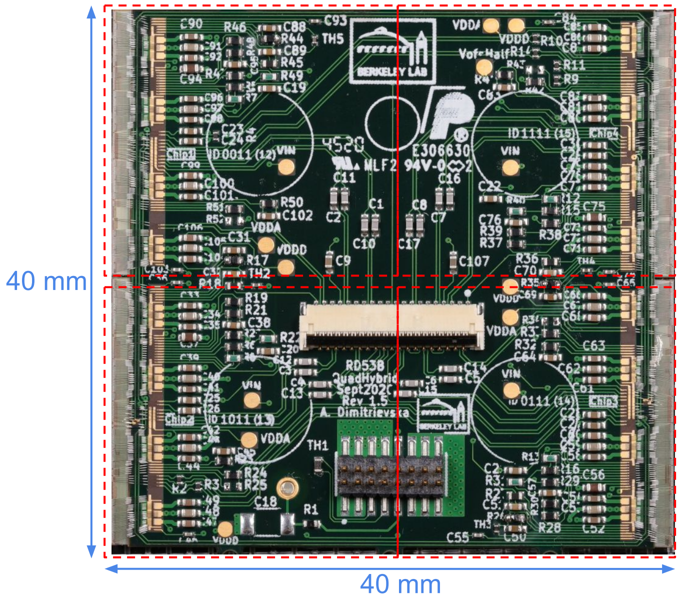


-> detector with small pixel size is required to achieve high resolution

ITk Pixel detector (ITkPix)

- ITkPix quad module
  - will be used in ATLAS pixel detector
  - single sensor + 4 readout asic + PCB
  - 400 x 384 pixels /asic
  - pixel size : 50 um x 50 um





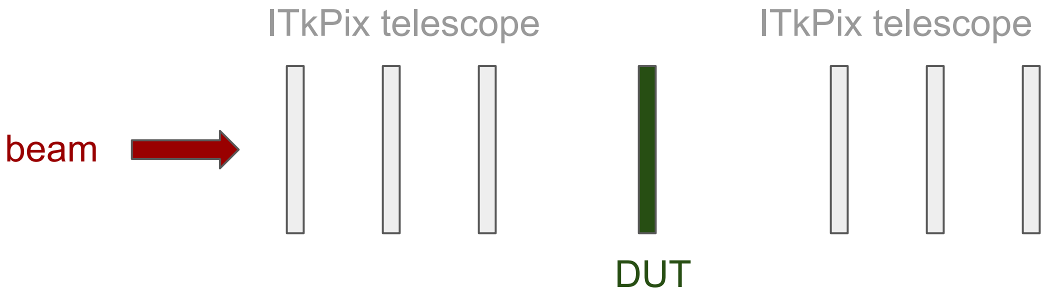
Motivation

- develop high resolution telescope using ITkPix
  - pixel size of ITkPix : 50 um x 50 um
  - resolution : d = 50 um

    $\sigma_x \sim 14.4$ um

ITkPix telescope layout

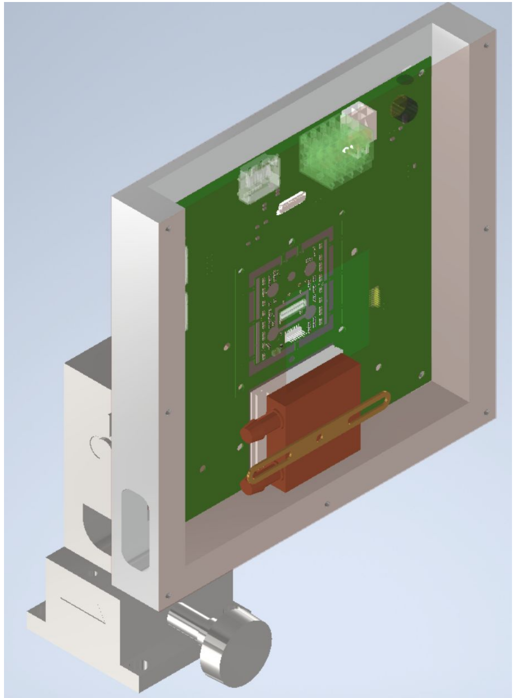
- ITkPix quad module
- 6 layers
- provide trigger for DUT using self trigger signal of ITkPix



⇨ current ITkPix PCB cannot readout self trigger signal
⇨ Objective : design new PCB for telescope

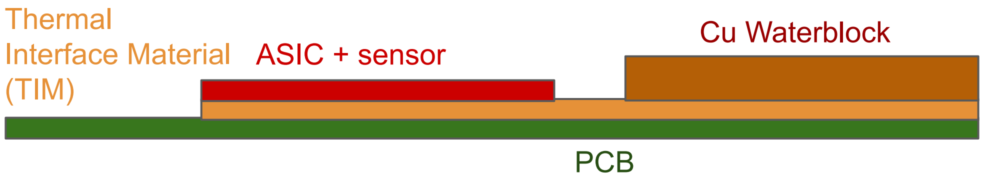
Design Requirements

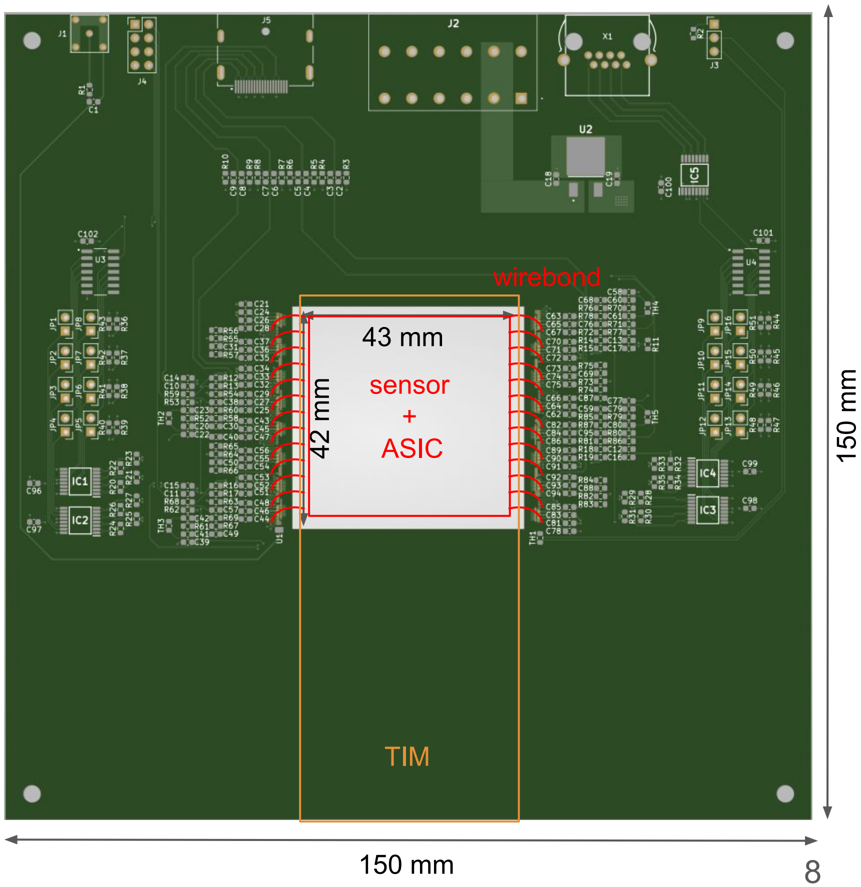
- low amount of material
- readout self trigger signal
- compatible with ITk telescope coolingbox
  - size : 150 mm x 150 mm
  - connectors on top
  - cooling block on bottom



Design telescope PCB

- sensor + asic wirebonded with PCB
- hole to reduce the amount of material
- space for cooling block

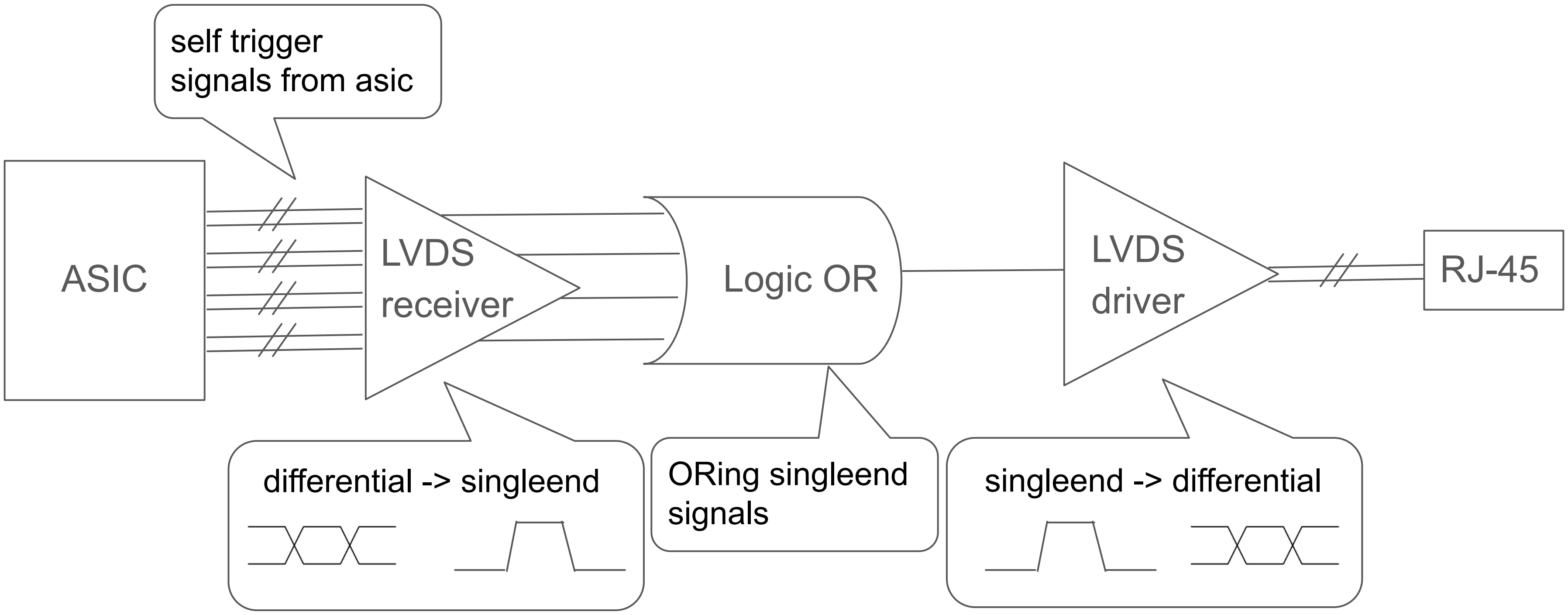




Functions of telescope PCB

- monitor temperature on the PCB
  - using negative temperature coefficient (NTC) thermistor
  - high temperature -> low resistance
- monitor voltage or current from the different part of chip
  - readout voltage multiplexer (MUX) from asic
- readout self trigger signal
  - next page

Self trigger readout schematics



Conclusion

- ❖ developing high resolution (σ_x ~ 14.4 um) telescope system in test beamlines using ITkPix

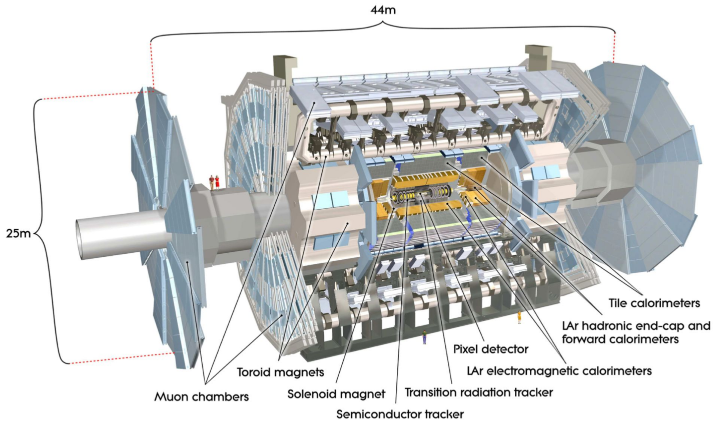
⇩

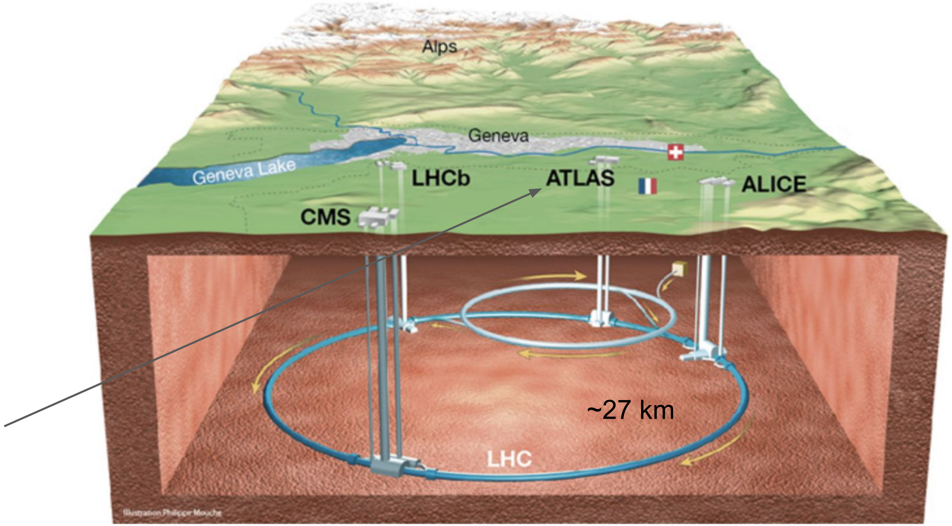
- ❖ designed PCB for telescope which can readout self trigger

Back Up

ATLAS detector

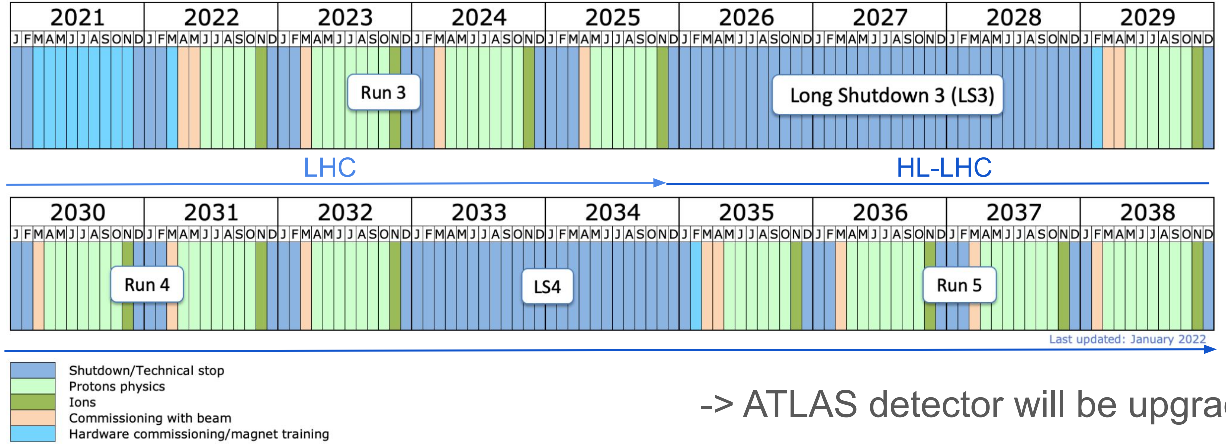
- ❖ LHC (Large Hadron Collider)
  - ➢ world's largest and highest energy particle collider built by CERN
  - ➢ bunches of up to 10^{11} protons collide at 40 MHz
  - ➢ CM energy : 13-14 TeV
  - ➢ integrated luminosity : 300 fb^{-1} (run3)
- ❖ ATLAS detector
  - ➢ probe p-p collision





High-Luminosity LHC upgrade

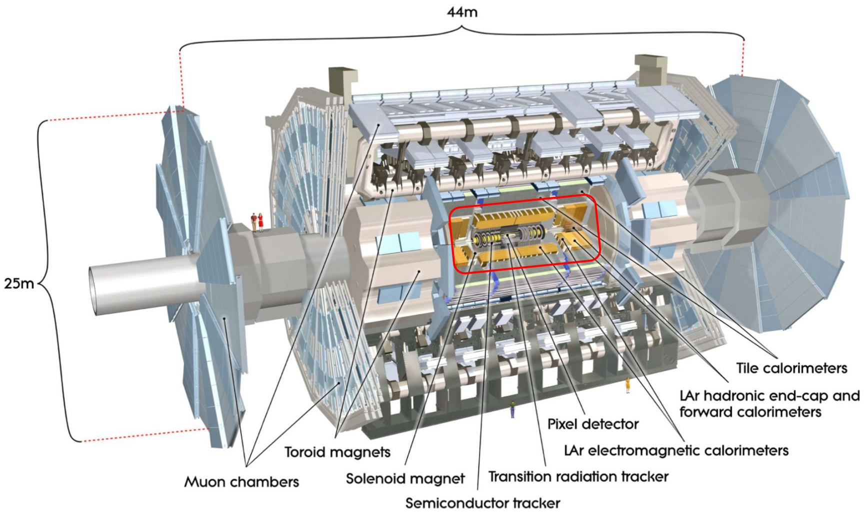
- ❖ HL-LHC upgrade
  - ➢ 2029~ operation
  - ➢ integrated luminosity x10
  - ➢ the higher luminosity, the more data
    - ■ study known mechanisms in greater detail
    - ■ observe new rare processes

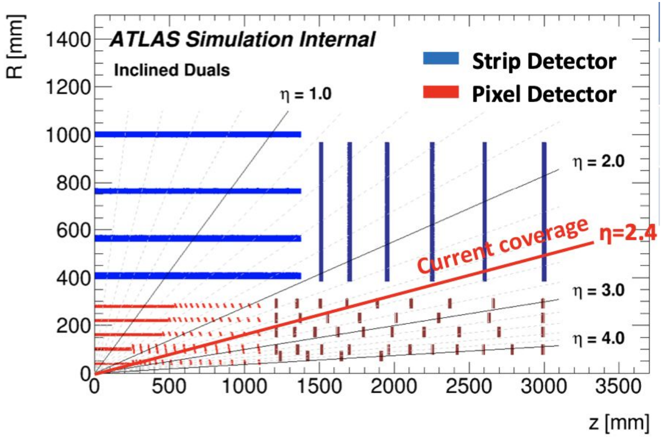


-> ATLAS detector will be upgraded

ATLAS Inner Tracker

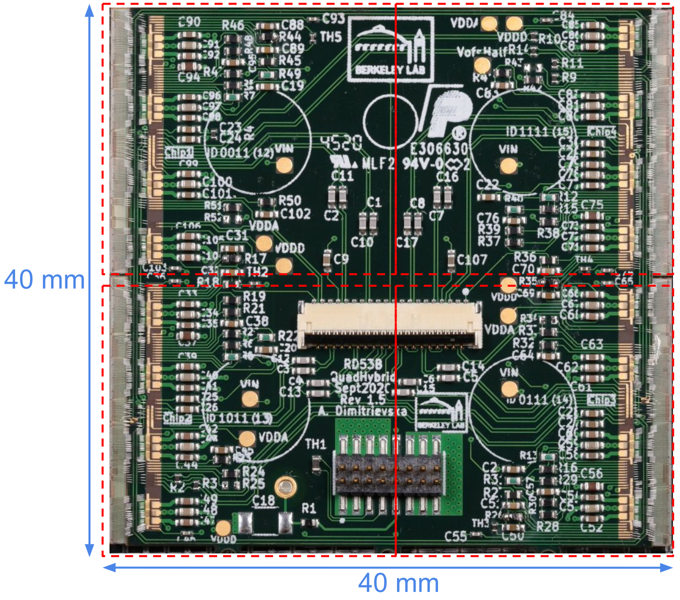
- ATLAS ITk
  - ATLAS Inner Detector (ID) will be upgraded to ATLAS Inner Tracker (ITk)
    - ID : pixel + SCT(strip) + TRT(chamber)
    - ITk : all silicon semiconductor tracker
  - larger coverage area
    - pixel : 2.7 m^2 -> 8.2 m^2
    - strip : 34 m^2 -> 165 m^2
  - higher forward coverage
    - η<2.5 -> η<4.0

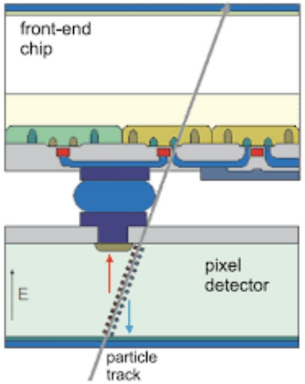


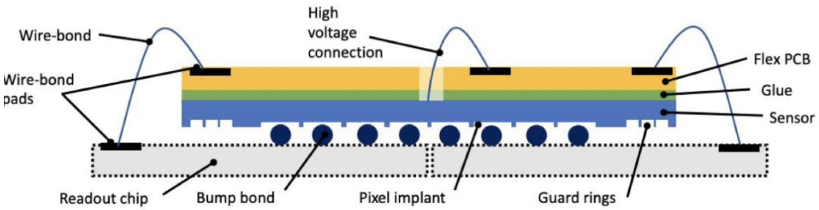


ITk Pixel detector (ITkPix)

- ITkPix quad module
  - will be used in ATLAS pixel detector
  - single sensor + 4 frontend asic + flex PCB
  - size : 40 mm x 40 mm
    20 mm x 20 mm (ASIC)
  - 400 x 384 pixels in one asic
  - pixel size : 50 um x 50 um



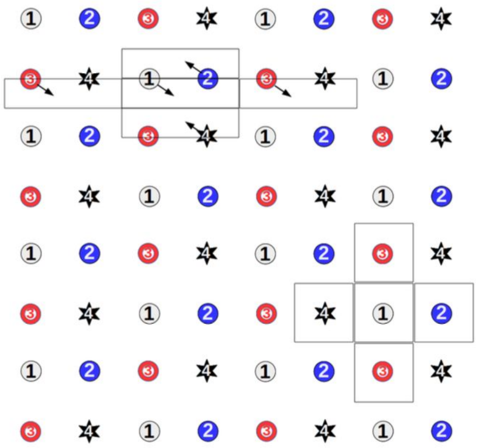


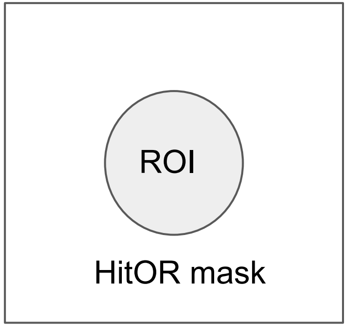


HitOR bus

- pixels are grouped into the 4 HitOR busses (a chain of serially connected pixels)
- any pixel in the bus firing will cause the bus to go high
- HitOR busses used to register pixel hits and issue trigger to itself (self trigger)
- there is a configuration bit for each pixel to activate the pixel for the HitOR

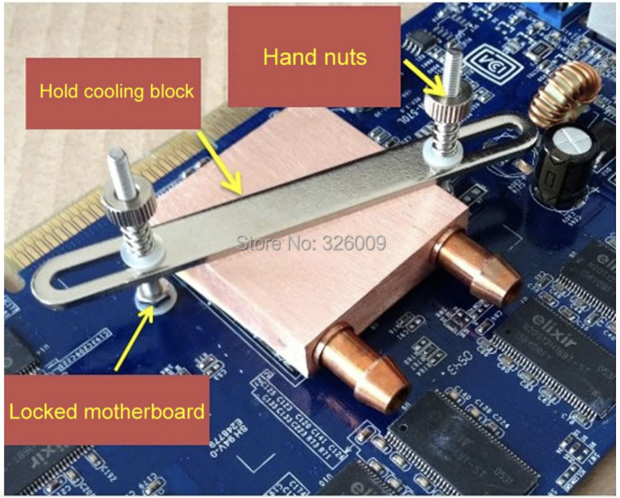
-> We can choose region of interest (ROI) by using HitOR bus

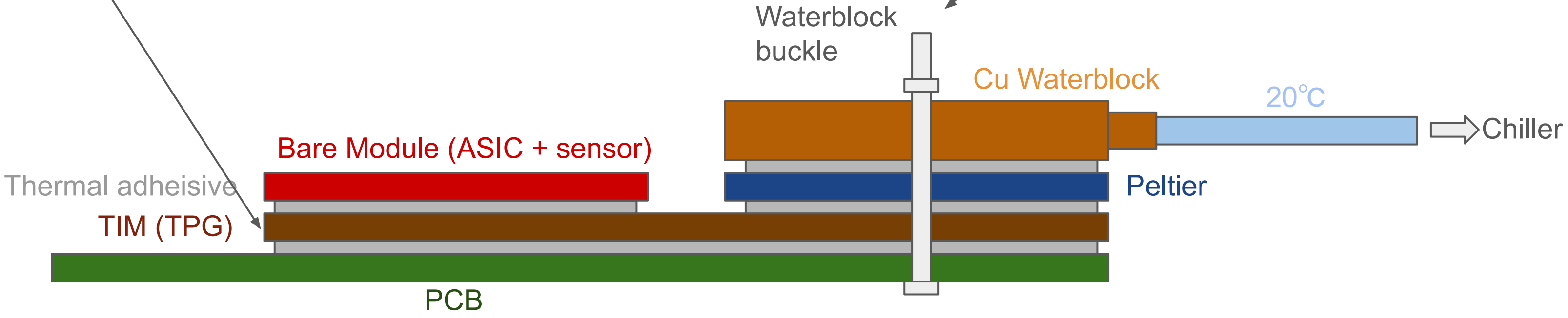




Thermal design

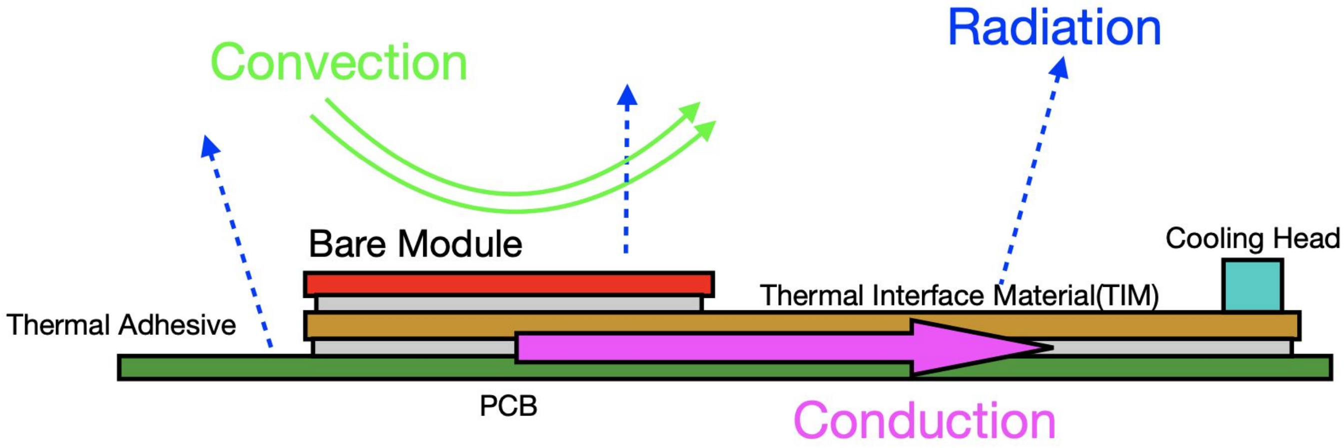
Material	In-Plane TC (W/m-K)	Thru-Plane TC (W/m-K)	In-Plane CTE (ppm/ºC)	Specific Gravity	Specific In-Plane TC[1]
Aluminum	218	218	23	2.7	81
Copper	400	400	17	8.9	45
AlSiC-12	180	180	11	2.9	62
CuW	185	185	8.3	15.2	12
Carbon/Carbon	400	40	-1.0	1.9	210
CVD Diamond	1100-1800	1100-1800	1-2	3.5	310-510
TPG Graphite	1500+	10	-1	2.3	650



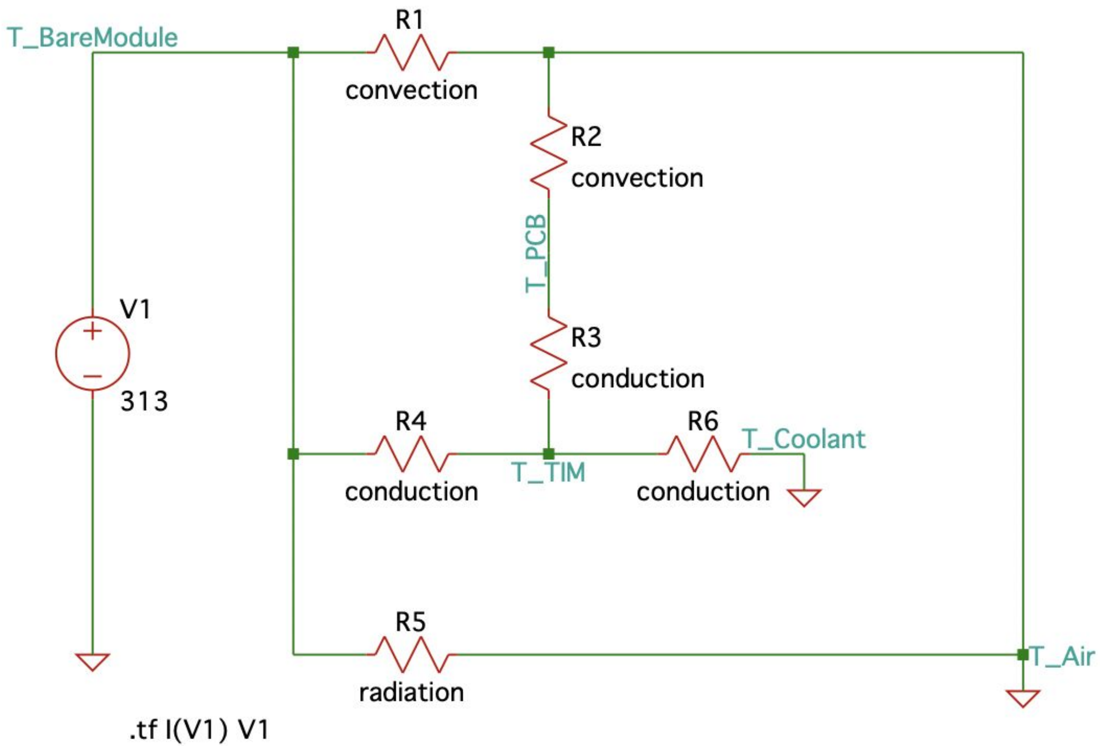


Thermal design

- heat dissipation
  - conduction
  - convection
  - radiation



Thermal network

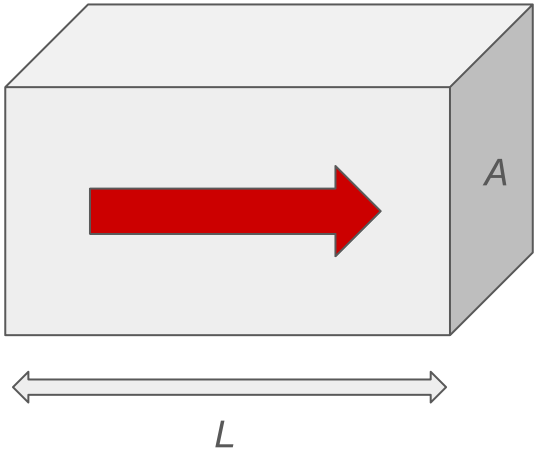


Conduction

- thermal conductivity :

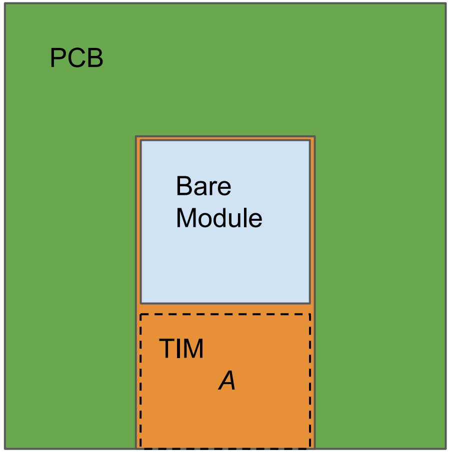
$$R = L / (\lambda \times A)$$

λ : thermal conductivity
A : surface area



Conduction

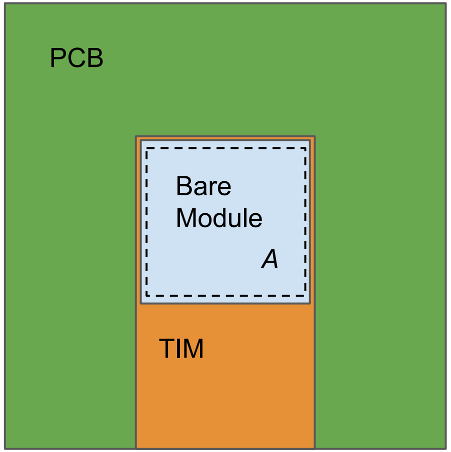
- R3 (TIM - PCB)
  λ = 2.3 W/mK (for adheisive)
  A = 43E-3 × 58E-3 = 2.494E-3 m^2
  L = 50E-6 m



R = 50E-6 / (2.3 × 2.494E-3) ~ 8.72E-3 K/W

Conduction

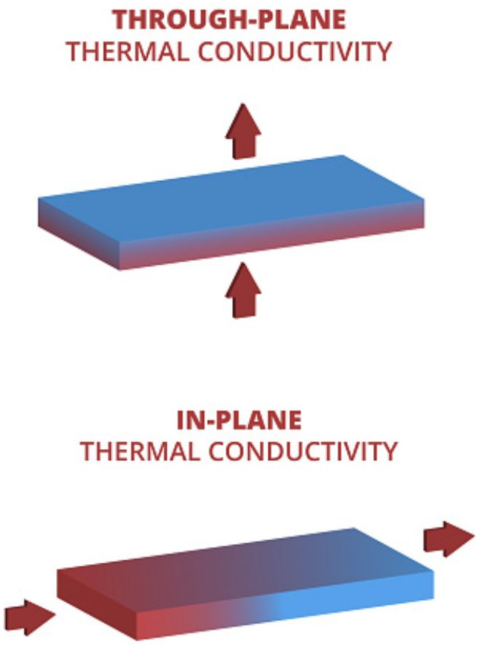
- R4 (Bare Module - TIM)
  λ = 2.3 W/mK (for adheisive)
  A = 40E-3 × 42E-3 = 1.68E-3 m^2
  L = 50E-6 m



R = 50E-6 / (2.3 × 1.68E-3) ~ 0.0129 K/W

TIM

Material	In-Plane TC (W/m-K)	Thru-Plane TC (W/m-K)	In-Plane CTE (ppm/°C)	Specific Gravity	Specific In-Plane TC[1]
Aluminum	218	218	23	2.7	81
Copper	400	400	17	8.9	45
AlSiC-12	180	180	11	2.9	62
CuW	185	185	8.3	15.2	12
Carbon/Carbon	400	40	-1.0	1.9	210
CVD Diamond	1100-1800	1100-1800	1-2	3.5	310-510
TPG Graphite	1500+	10	-1	2.3	650

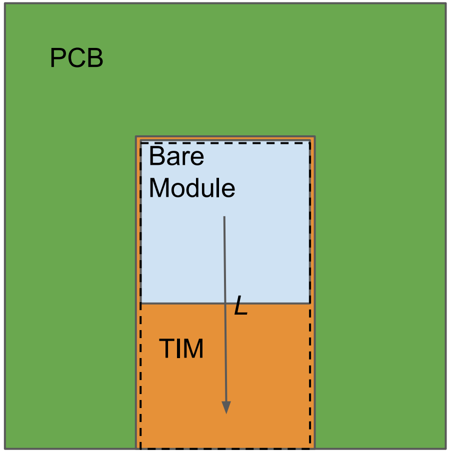


http://s262196942.onlinehome.us/ArchivedMeetings/2008_Symp/G%20-%20Thermal%20Session/Thermal_Session_1.pdf

-> in-plane TC and thru-plane TC may differ.

Conduction

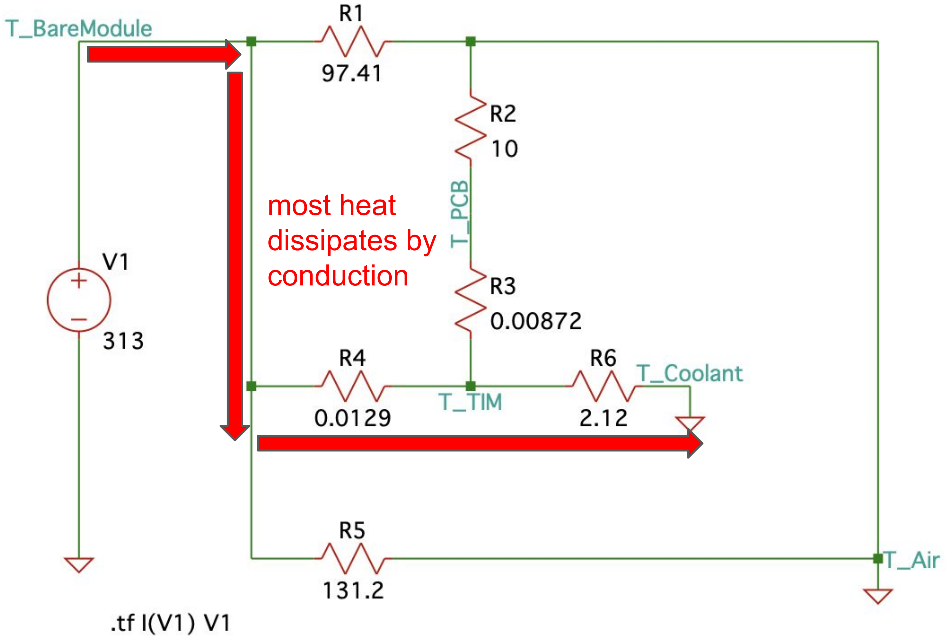
❖ R6 (TIM - Coolant)
λ = 1050 W/mK (for TC1050, maybe in-plane TC is much smaller)
A = 43E-3 × 0.5E-3 = 21.5E-6 m^2
L = 50E-3 m



R = 50E-3 / (1050 × 22.5E-6) ~ 2.12 K/W

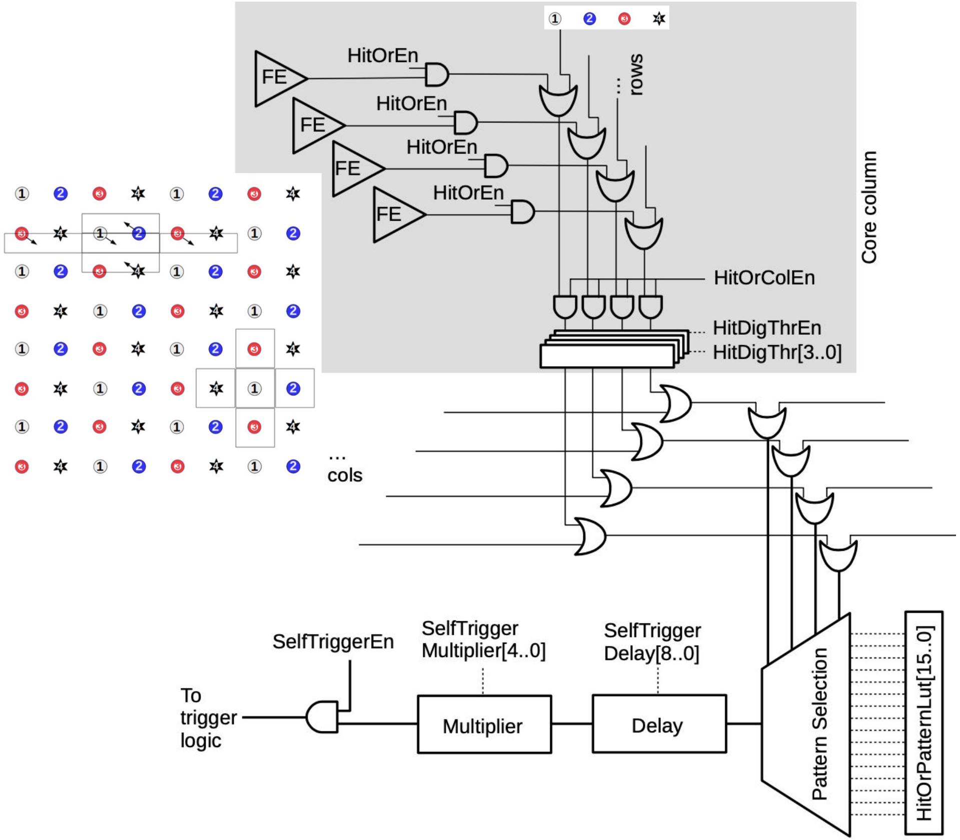
Thermal conductivity

- calculate input impedance using LTspice
- total thermal conductivity : 1.7085 K/W
- total heat dissipation :
  1.6V x 6A = 9.6 W
  ΔT = 1.7085 × 9.6
  = 16.4016 K

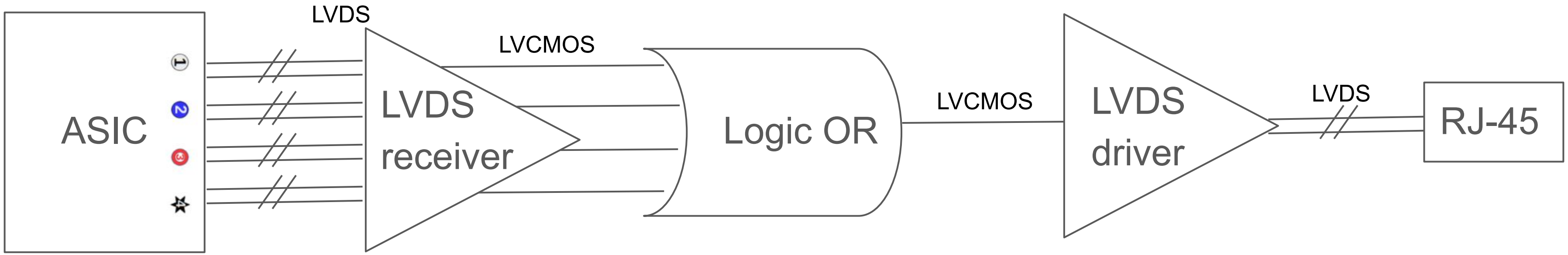


Self trigger

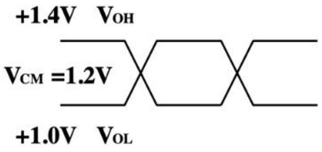
- 64 pixels in one core are grouped into the 4 OR networks
- HitOR busses used to register pixel hits and issue trigger to itself (self trigger)
- Has additional functionality (using the 4 different HitOr busses) to trigger on specific cluster patterns



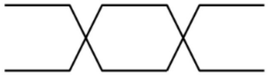
HitOR readout schematics



Problem : HitOR signal is not same as LVDS



typical LVDS

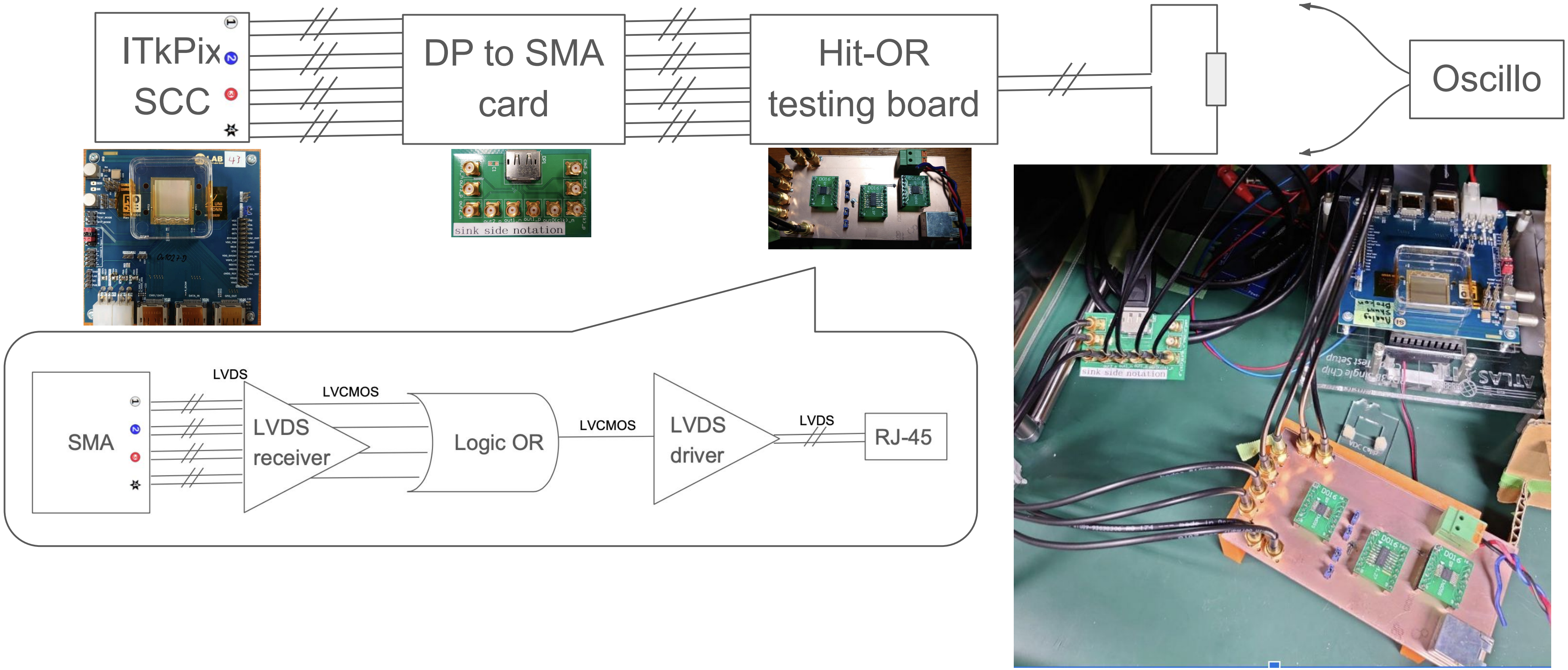


Vcm = ?

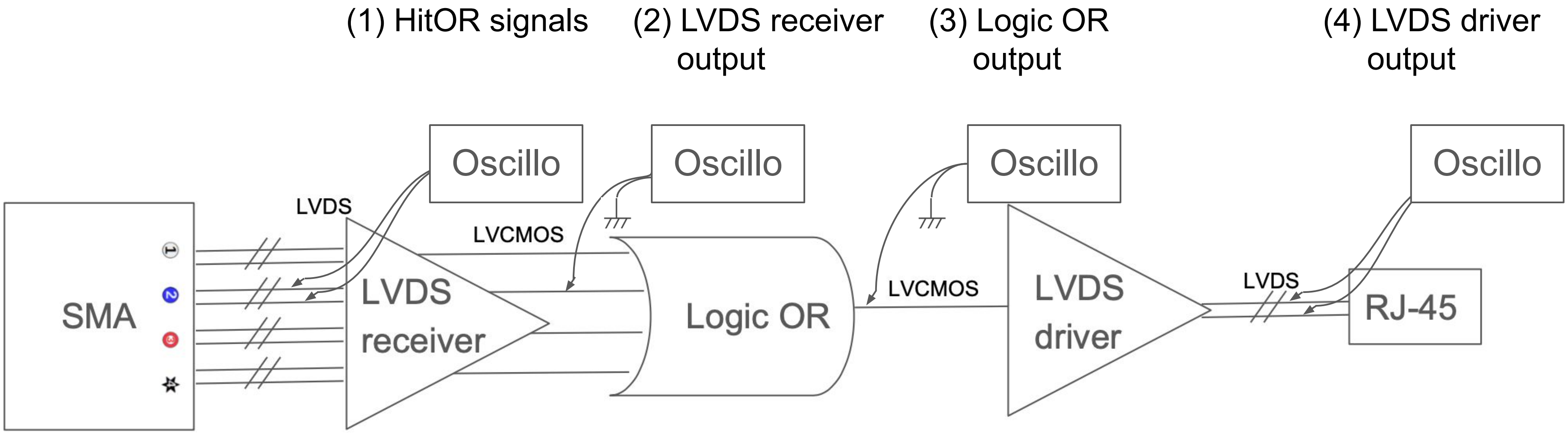
HitOR signal

-> we have to check if ICs works properly

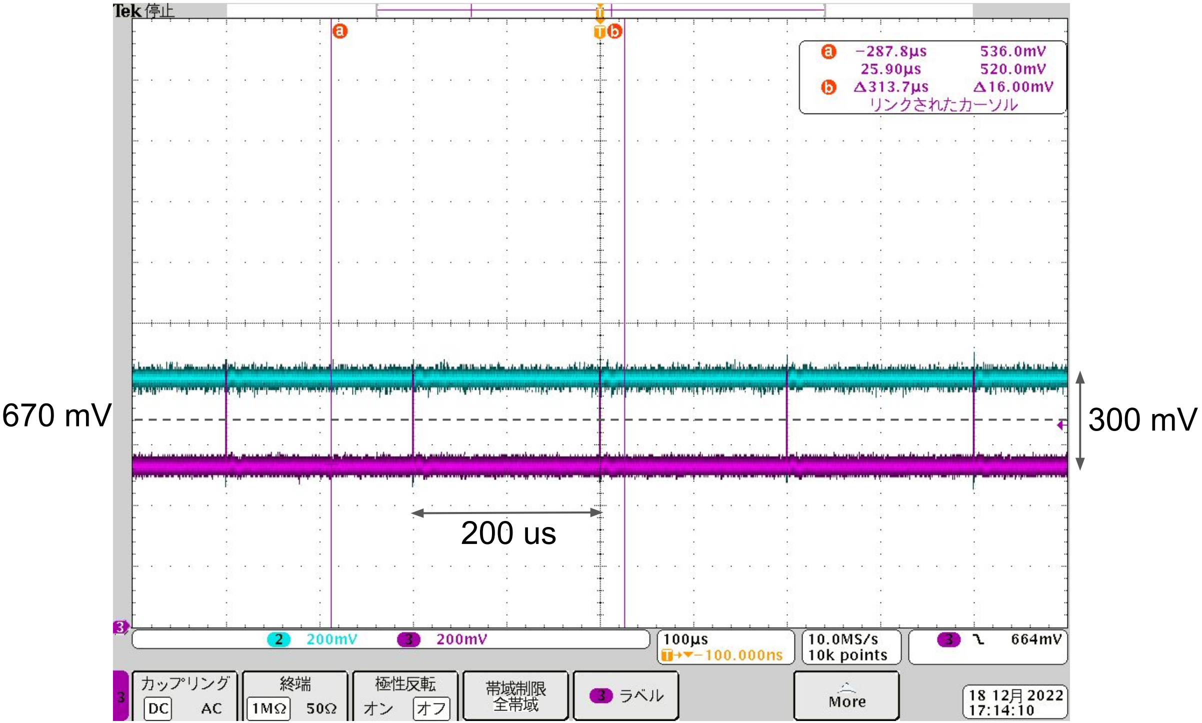
Hit-OR testing layout

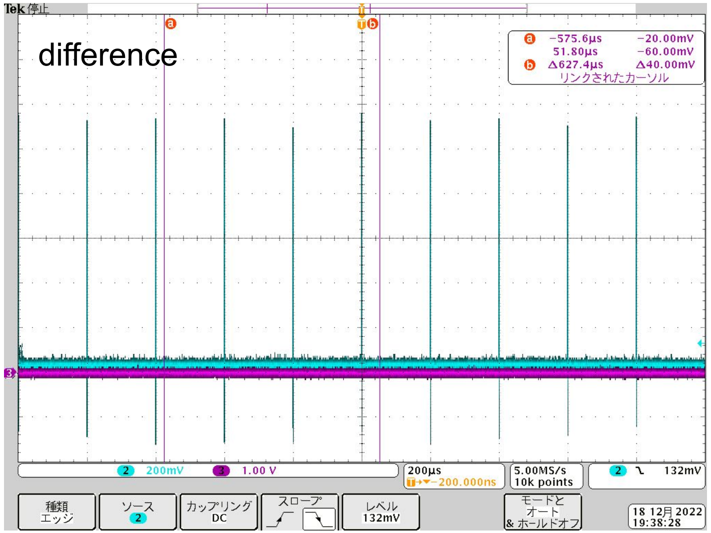


Probing point

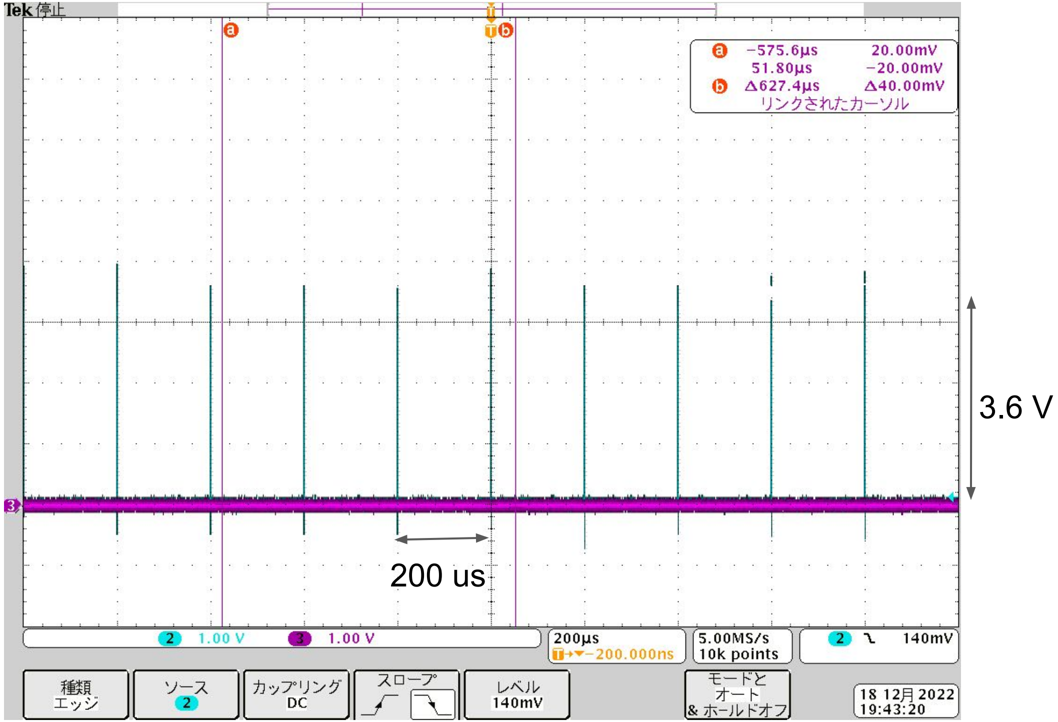


Results　(1) HitOR signals



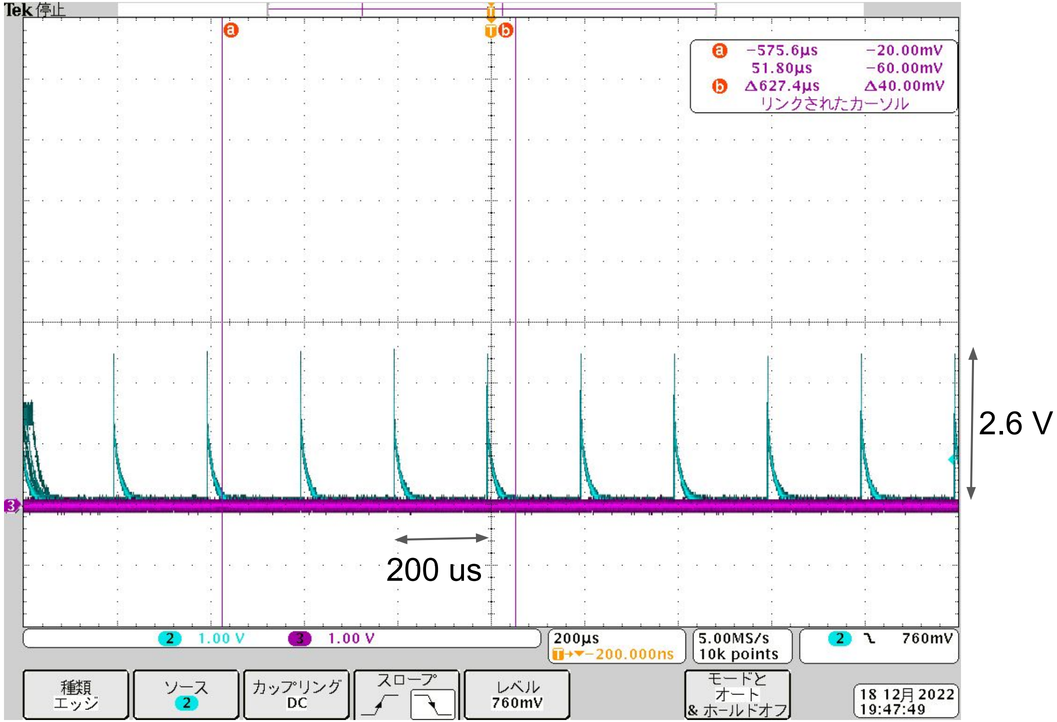


Results　(2) LVDS receiver output



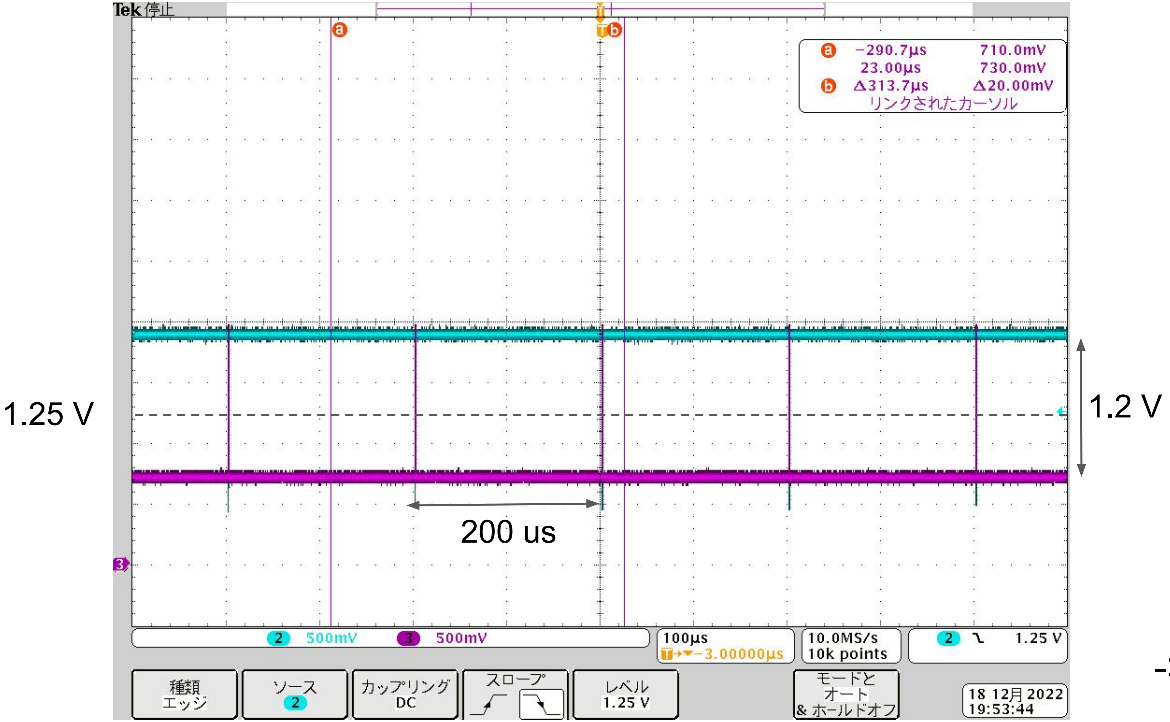
-> LVDS receiver worked properly

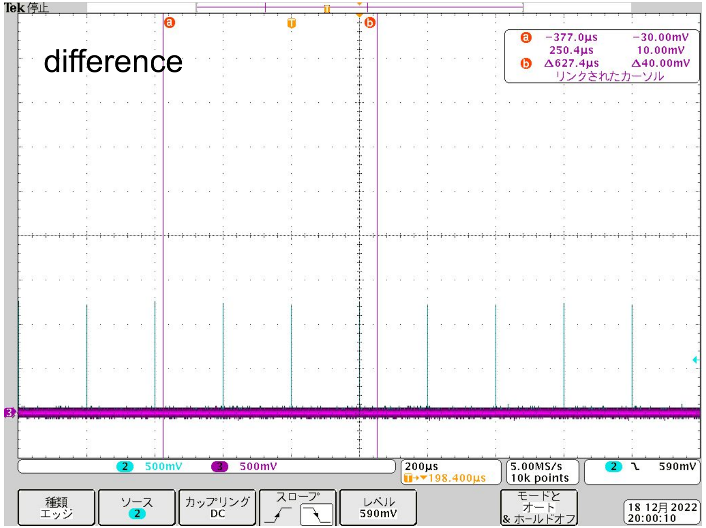
Results　(3) Logic OR output



-> Logic OR worked properly

Results (4) LVDS driver output

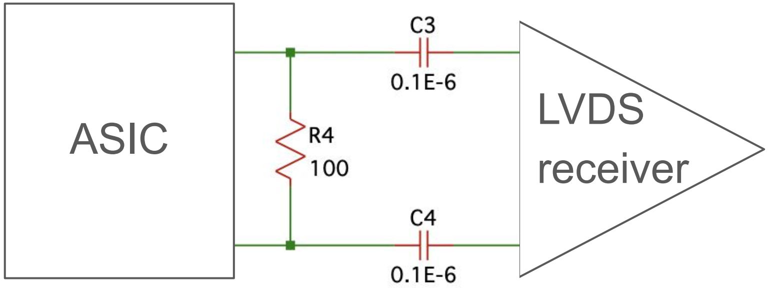




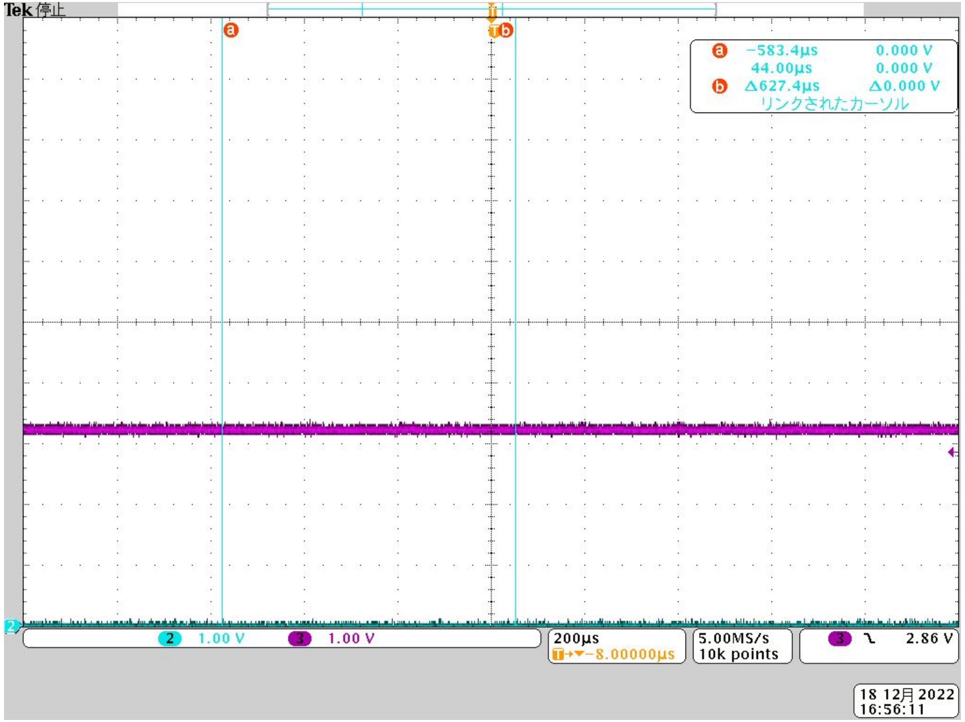
-> LVDS driver worked properly

HitOR testing with AC coupling

- AC coupled with 0.1uF condenser



Results　(2) LVDS receiver output



-> LVDS receiver didn't worked properly

HitOR signal is not dc balanced
-> supply bias voltage = 1.2v after AC couple