Development status of Ultra-low latency online event selection trigger system in COMET Phase - I

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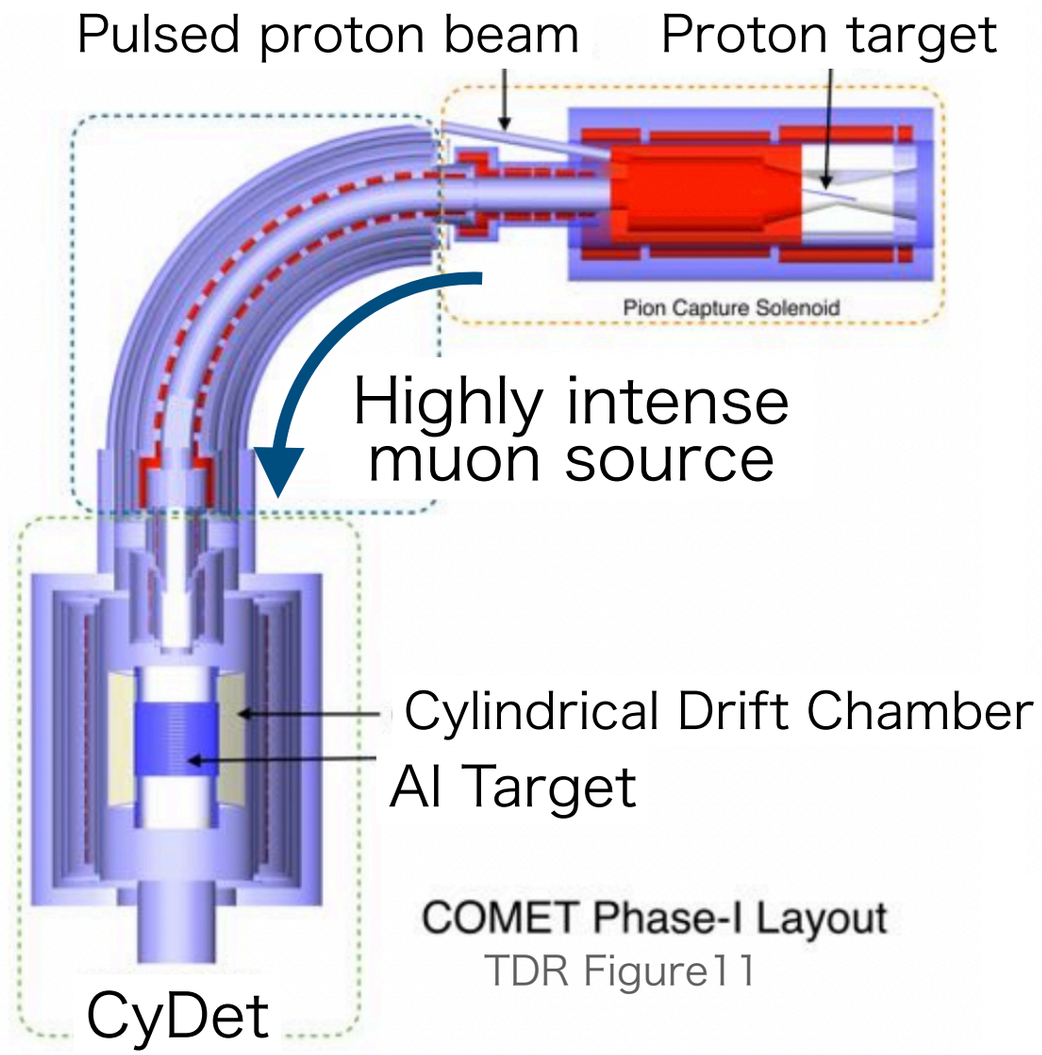
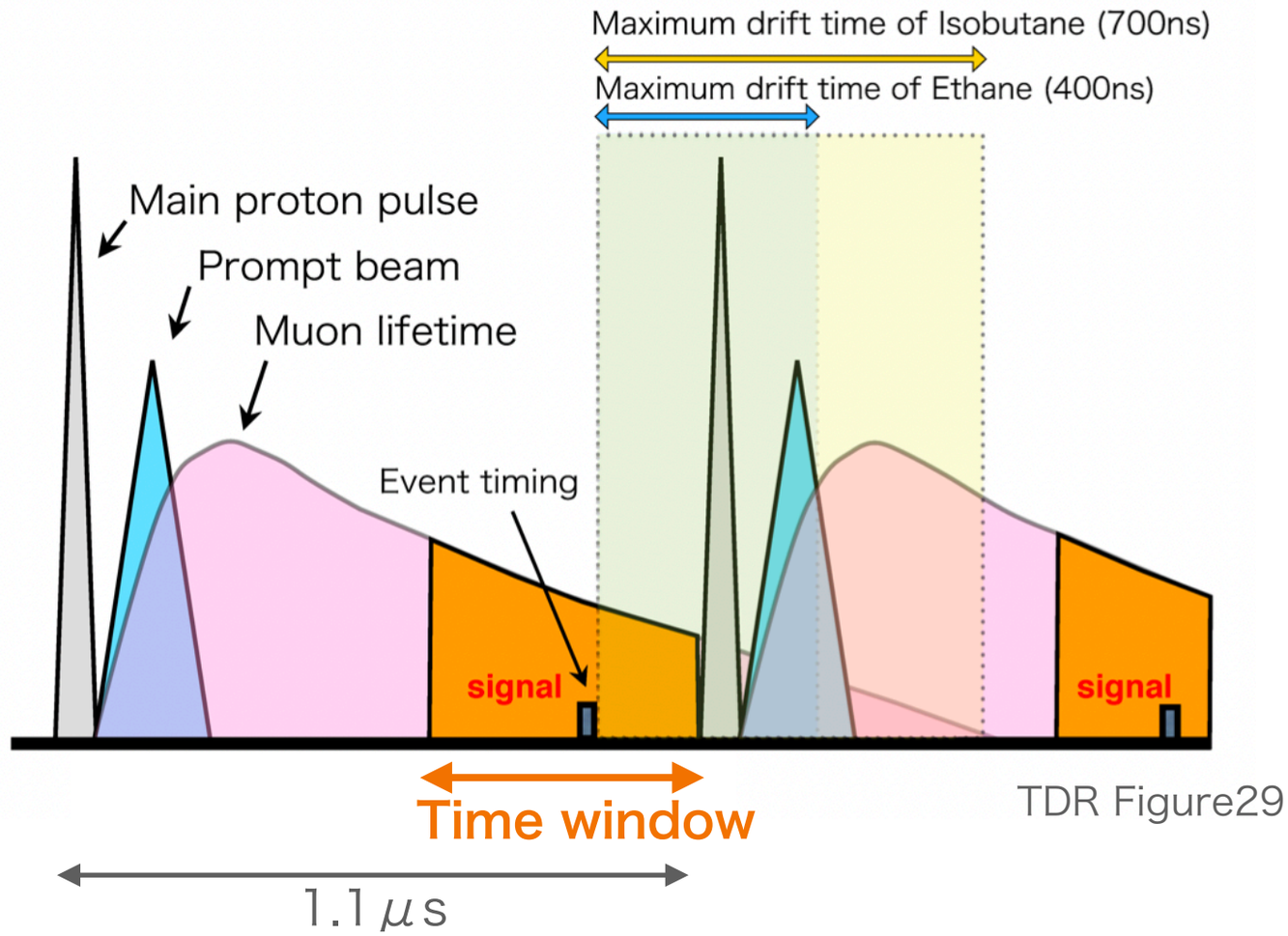
- COMET Phase-I
- Online trigger system
- CDC trigger chain test
- CyDet trigger chain test
- New online event classification algorithm

COMET Phase-I experiment



COMET Phase-I Layout
TDR Figure11



TDR Figure29

- **Purpose : Search for μ-e conversion in an Al target**
  - **Signal : monoenergetic 105 MeV electron**
- **Single event sensitivity :** 3.0×10^{-15} (100 times the current sensitivity)
- **Detector : Cylindrical detector system**
  - electron momentum and timing measurements

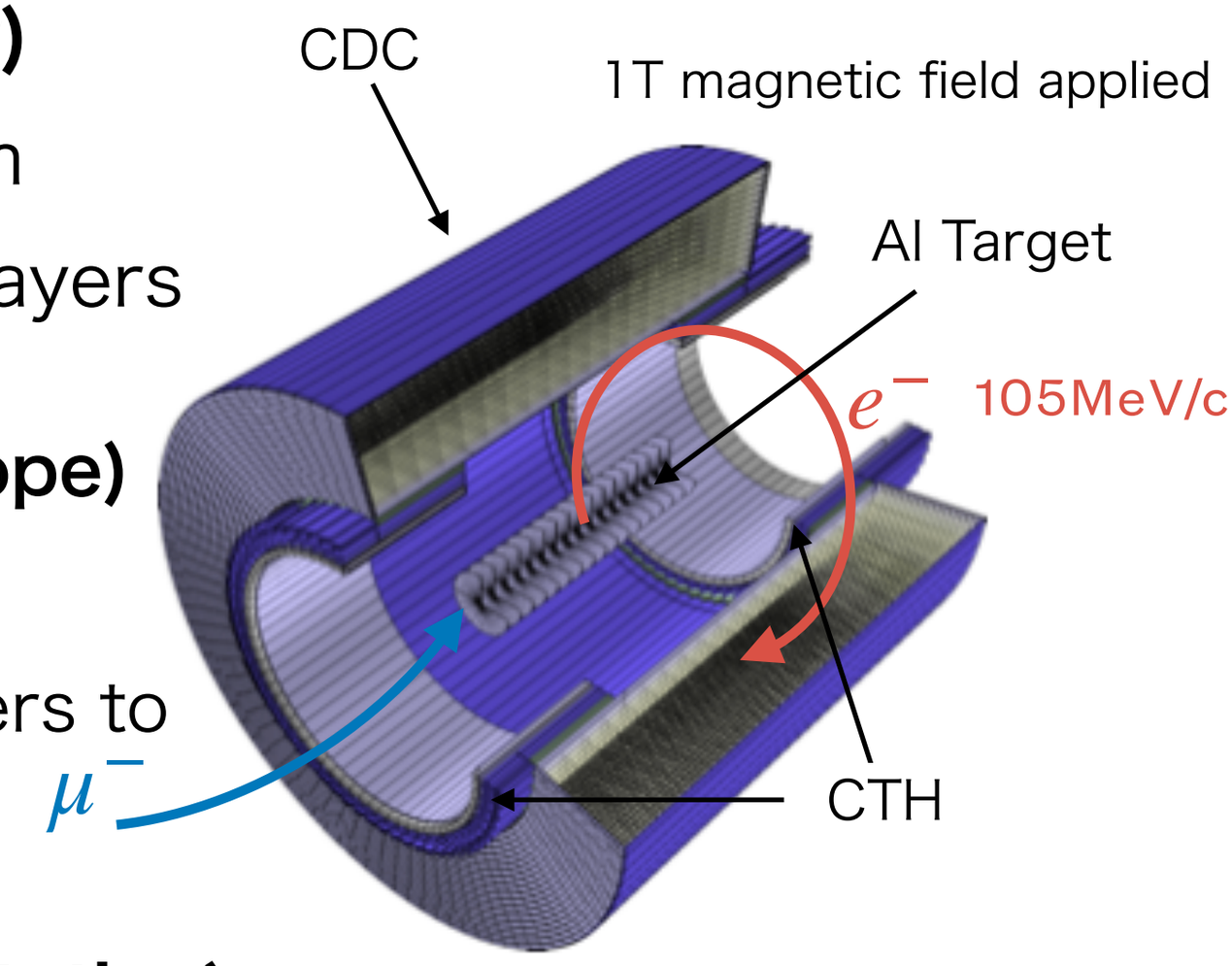
CyDet : Cylindrical detector system

CDC (Cylindrical Drift Chamber)

- Measure the particle momentum
  - 4986 sense wires, 20 stereo layers

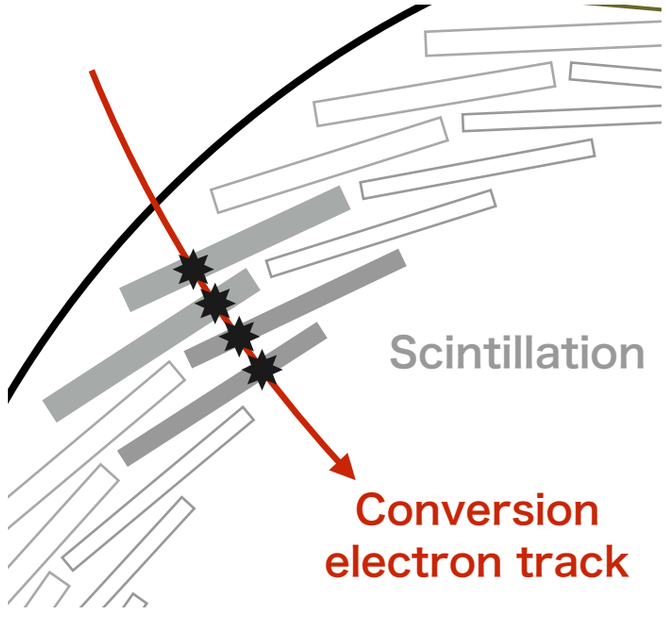
CTH (Cylindrical Trigger Hodoscope)

- Measure the electron timing
- Double layered Scintillation counters to make a primary trigger signal

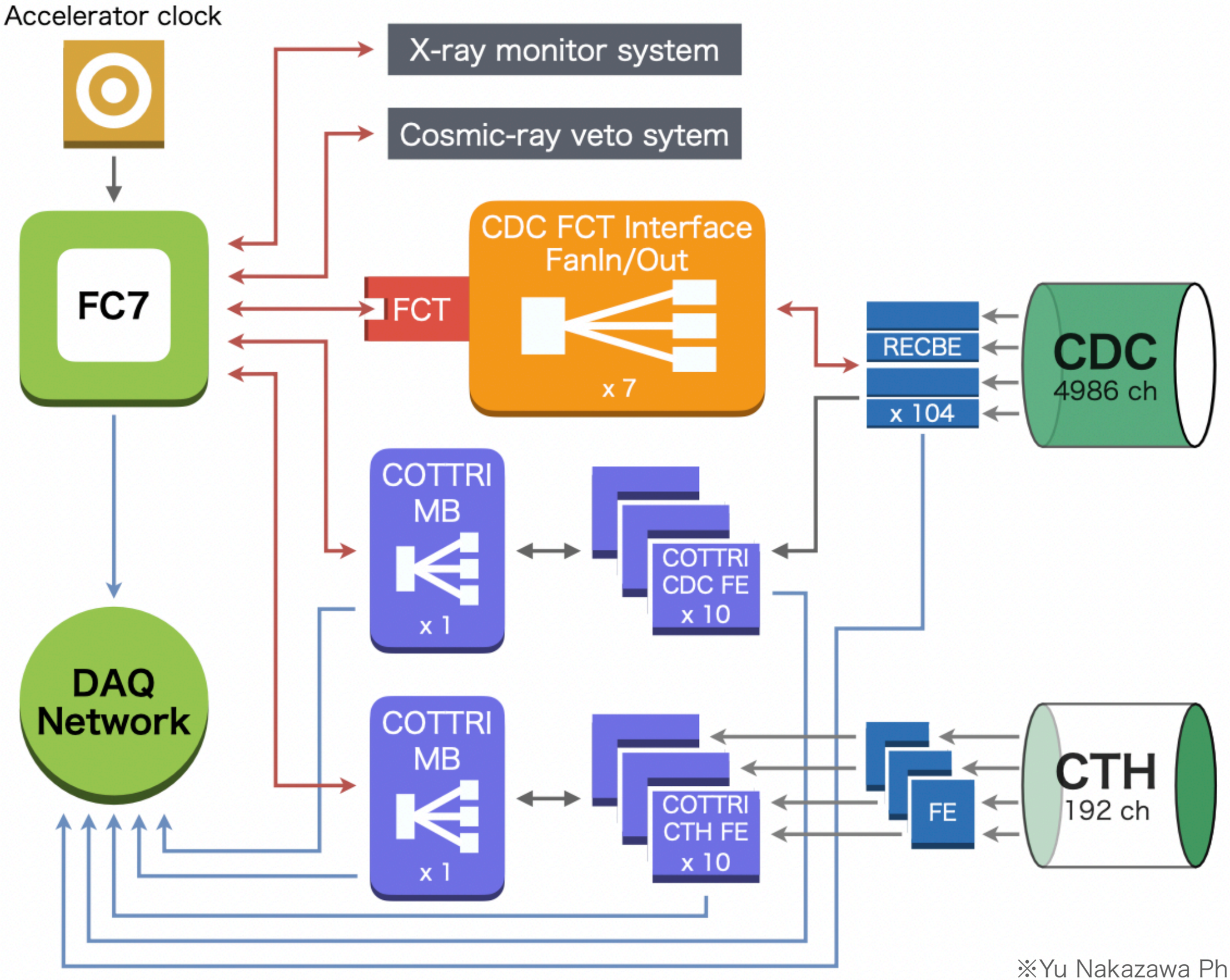


CTH trigger rate ~ 91 kHz (expectation)

- 4 fold coincidence
- low-E electron dominant

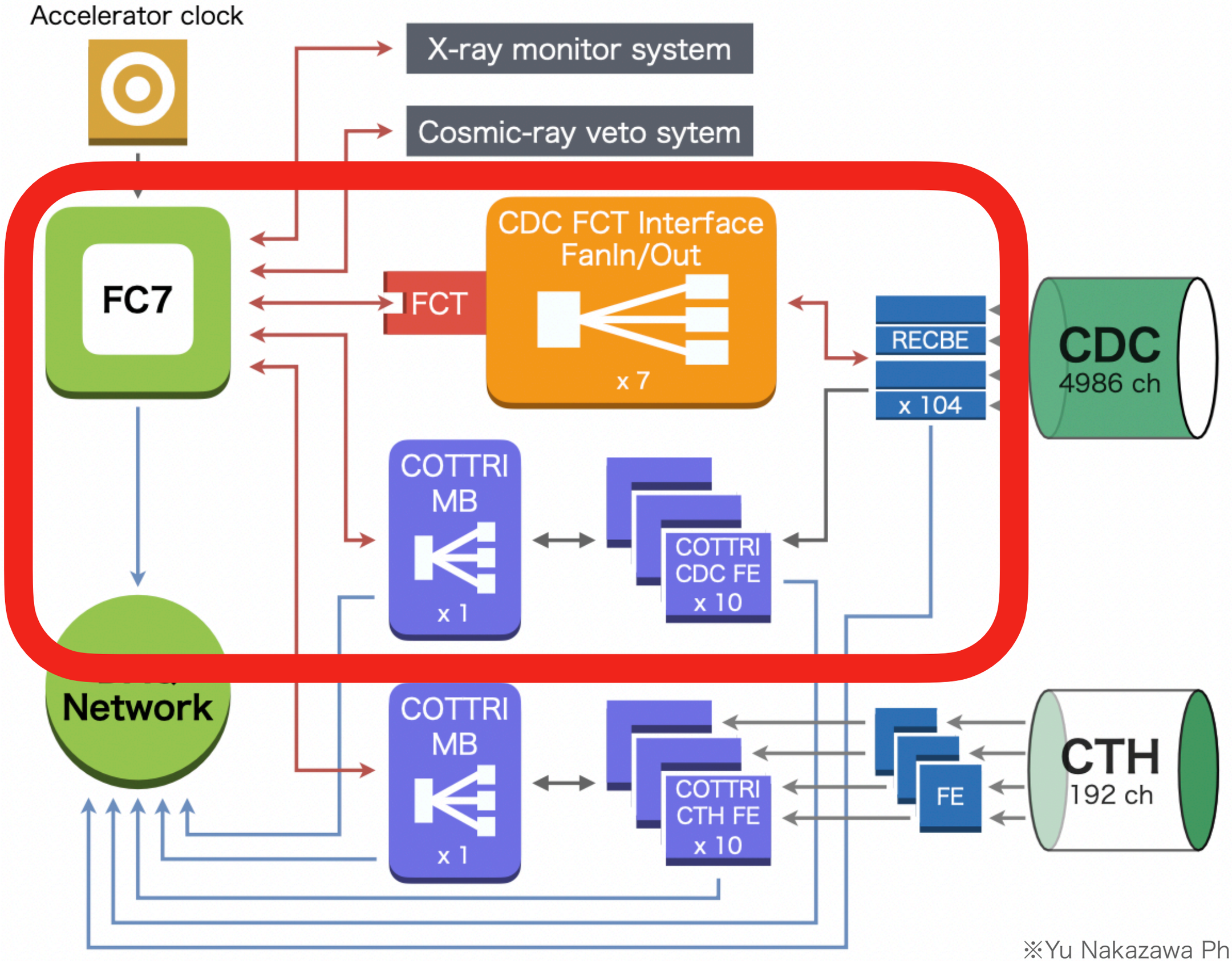


Online trigger system



※Yu Nakazawa PhD Thesis Fig2.12

Online trigger system



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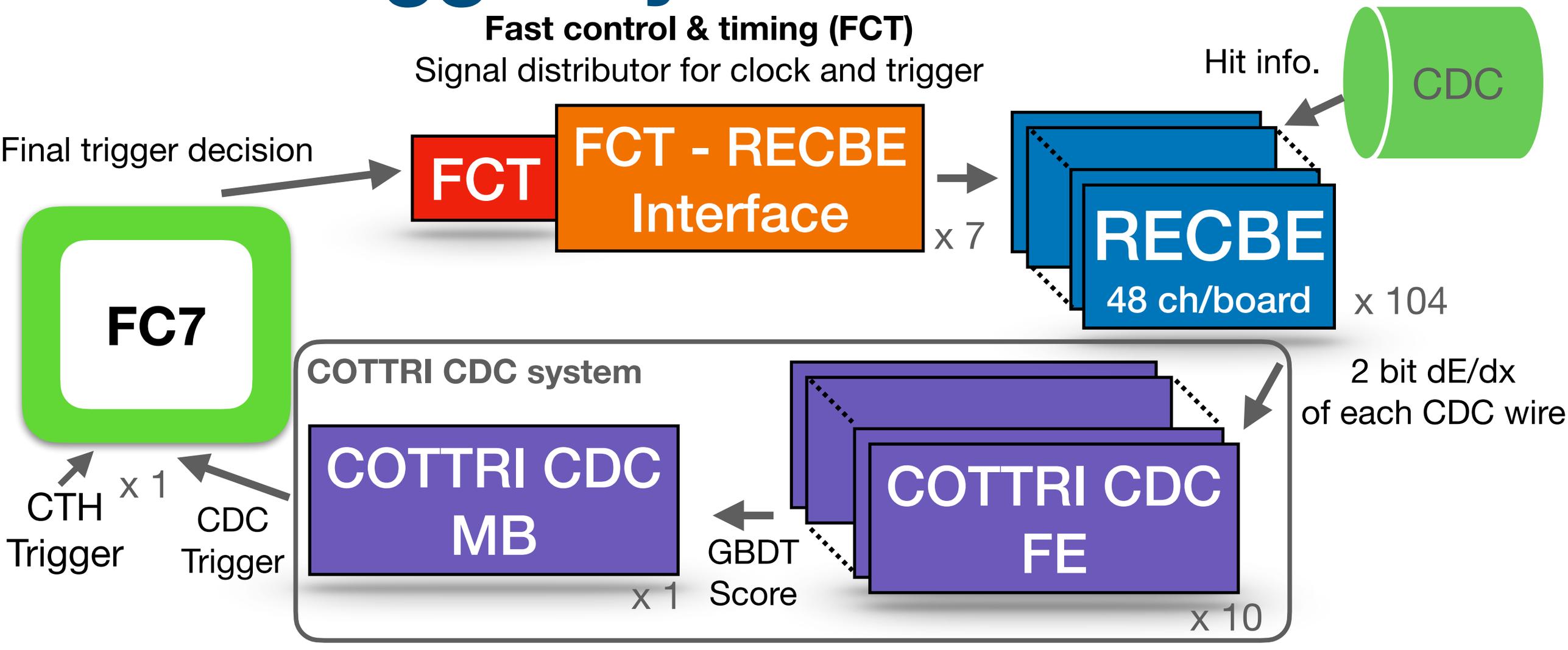
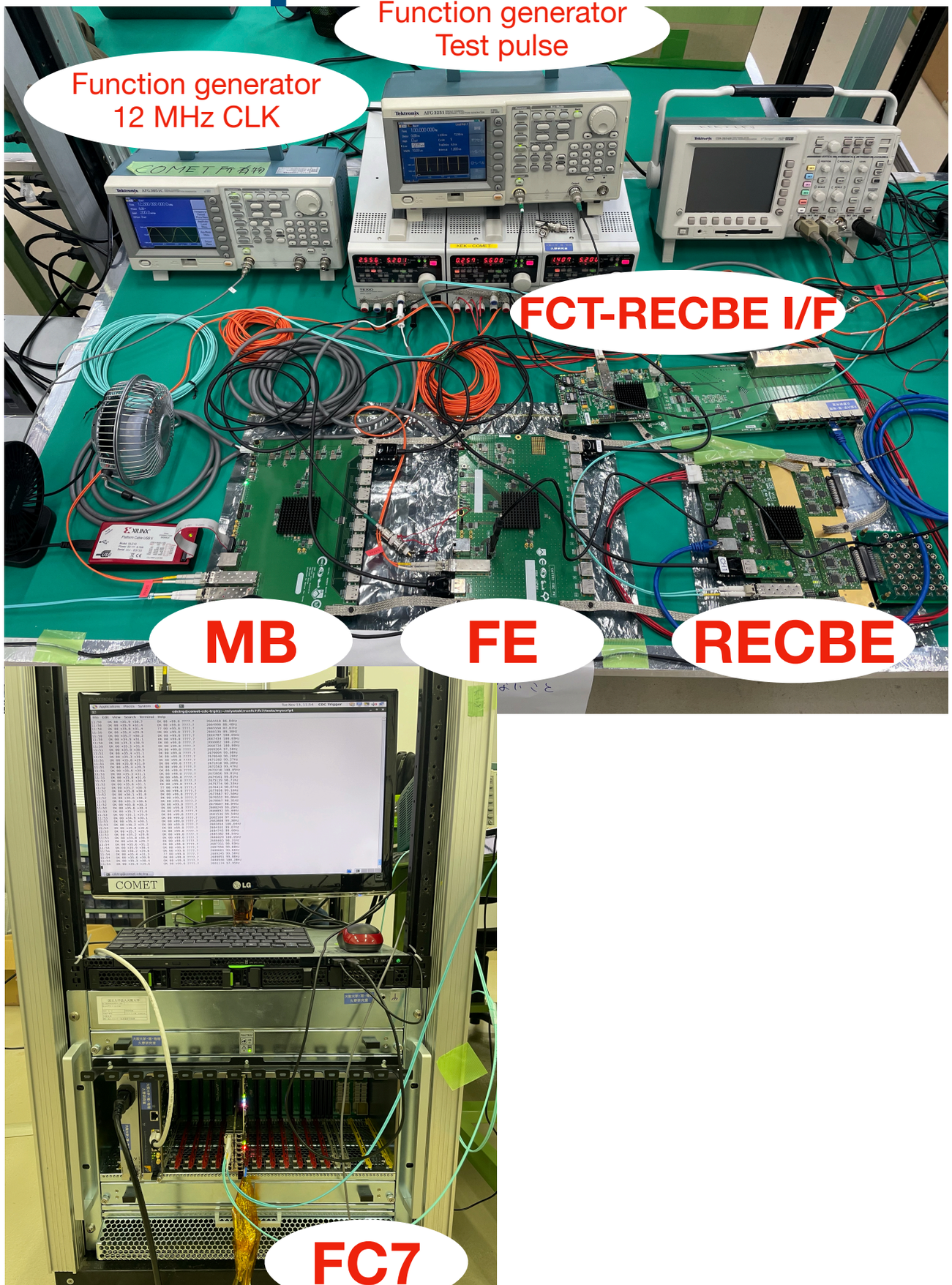
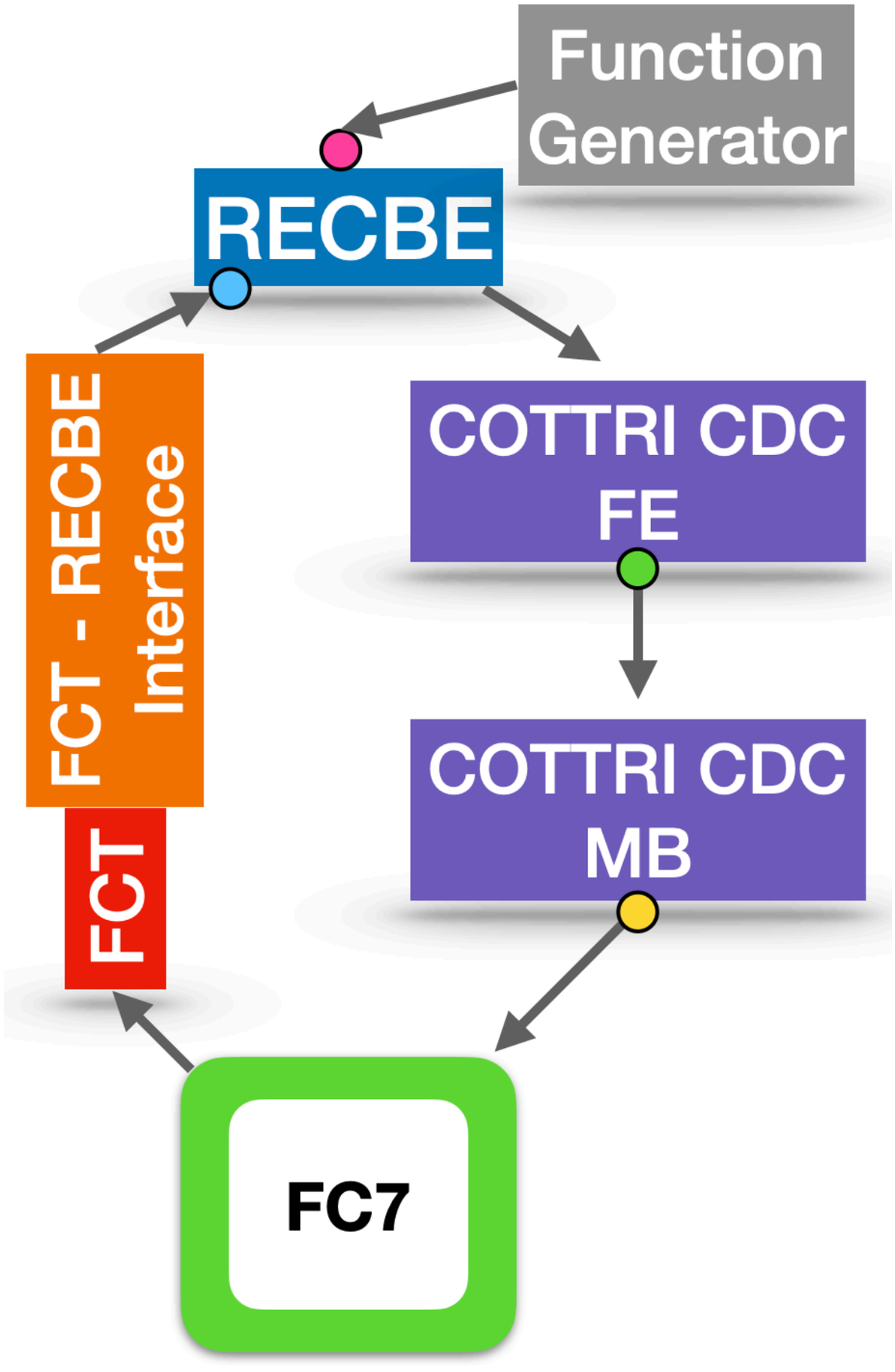
Online trigger system



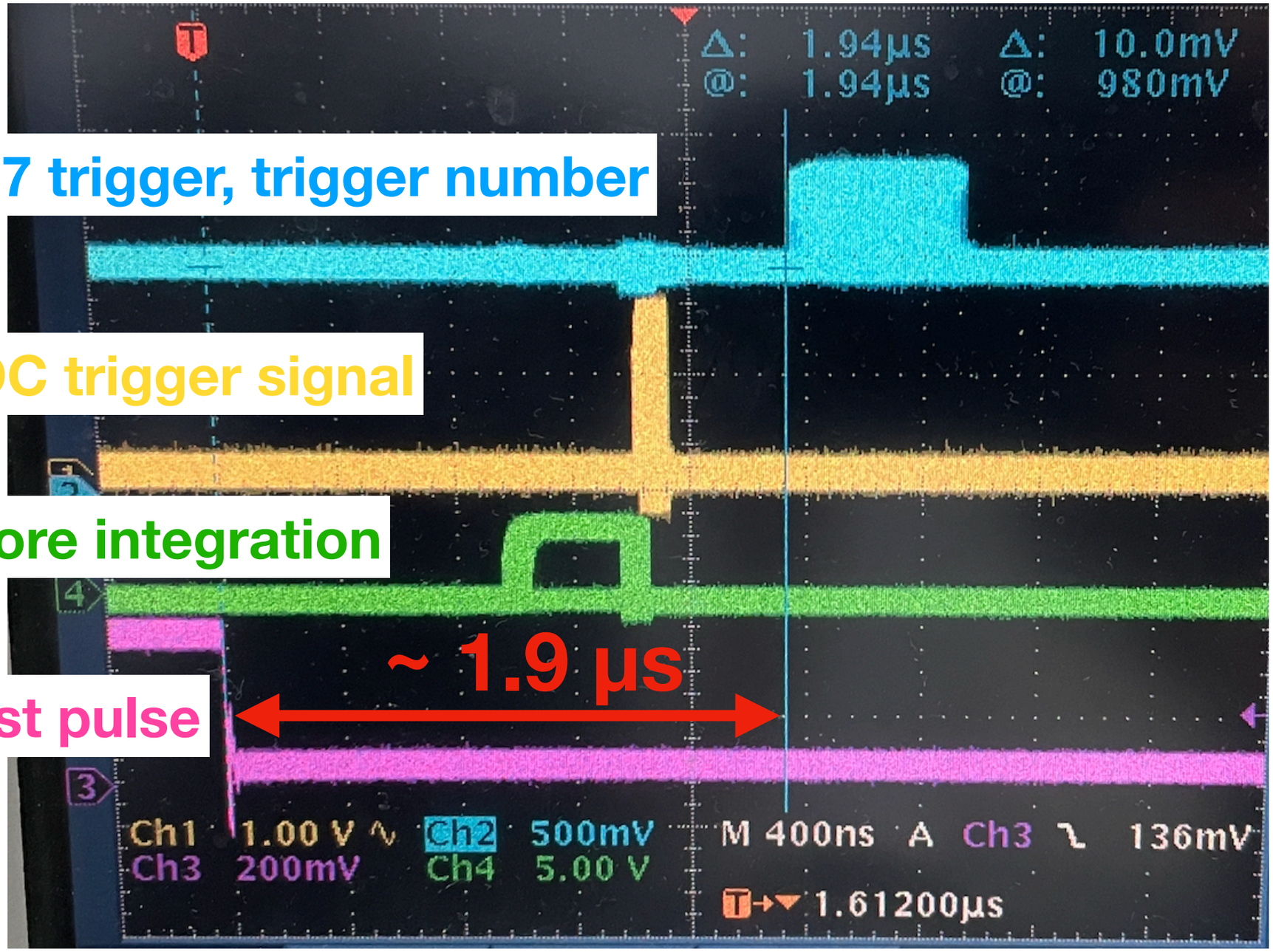
- RECBEs generate the 2 bit dE/dx information and send it @10 MHz
- COTTRI CDC system
  - FE : hit classification based on local/neighboring features.
    - Convert 2 bit data to GBDT scores in 400 ns integration time window
  - MB : event classification with the global feature.
    - Sums up the GBDT scores and makes the CDC trigger decision @10 MHz

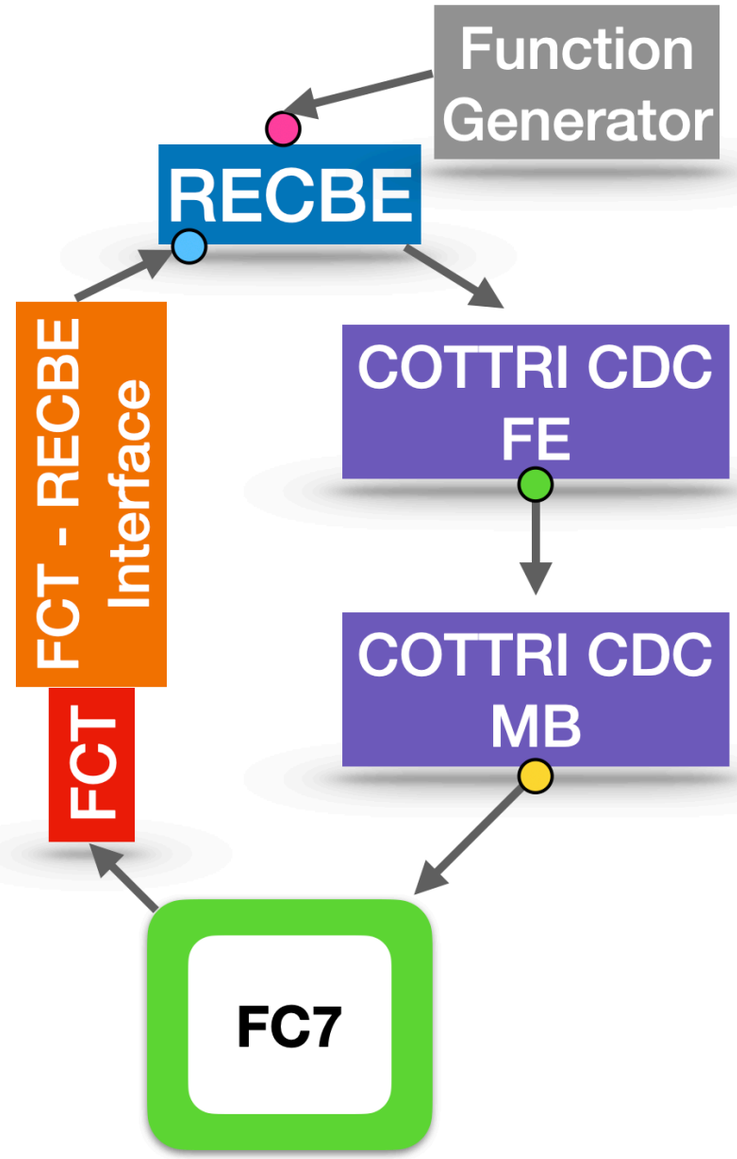
Set up


Function generator
Test pulse
Function generator
12 MHz CLK
FCT-RECBE I/F
MB
FE
RECBE
FC7


Function Generator
RECBE
FCT - RECBE Interface
FCT
COTTRI CDC FE
COTTRI CDC MB
FC7

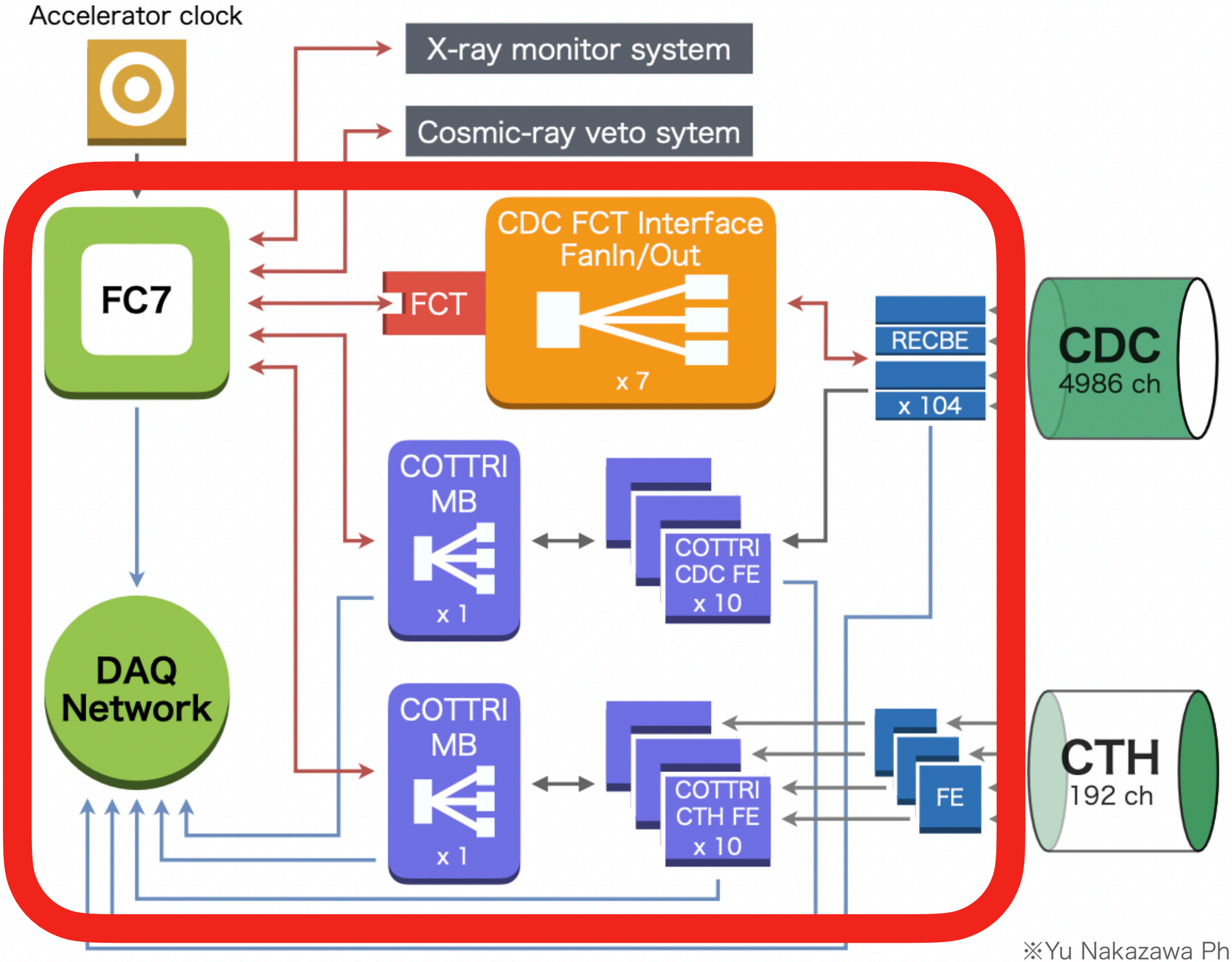
Latency measurement





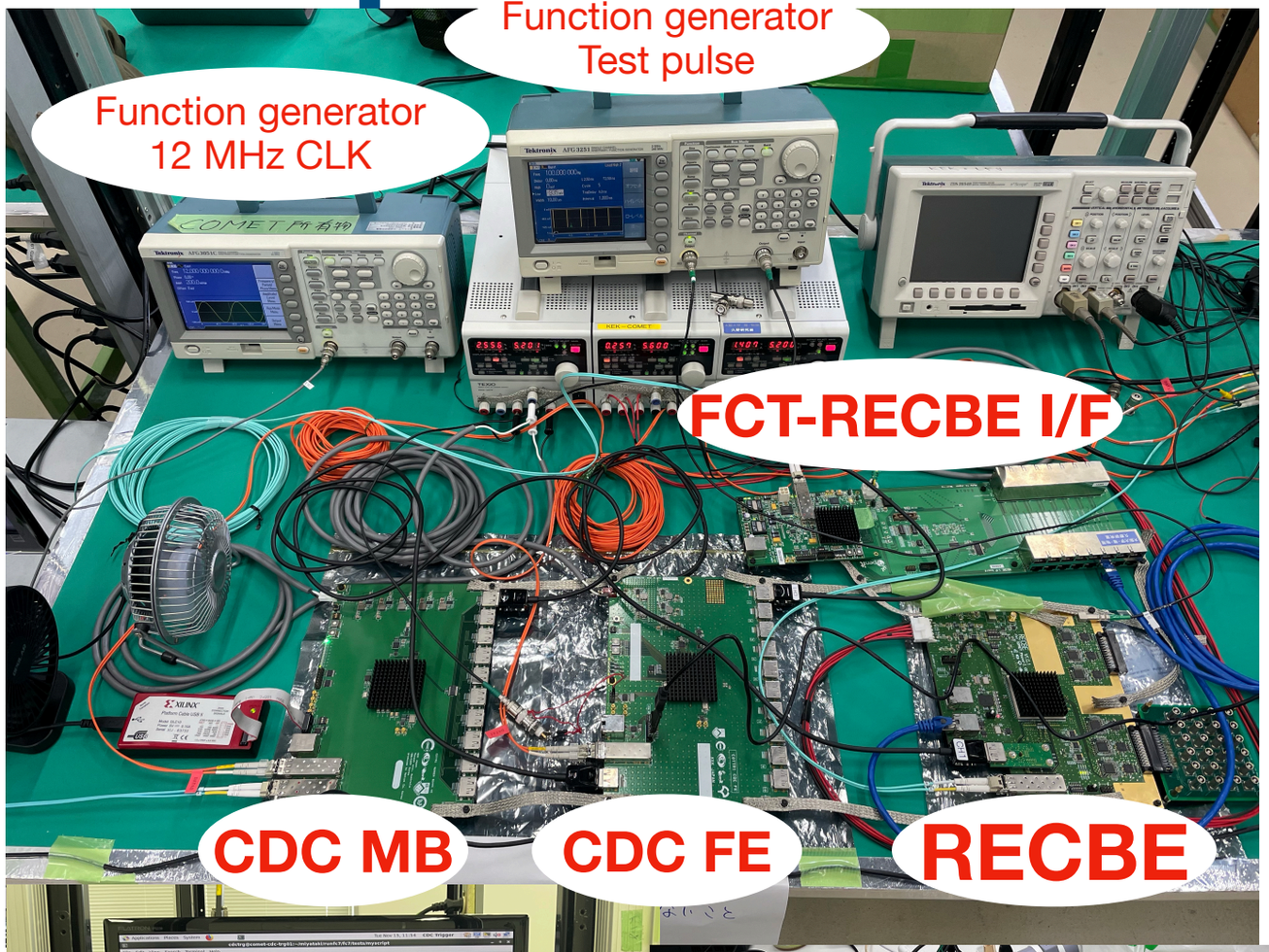
Latency (RECBE - COTTRI CDC system - FC7 - FCT・RECBE I/F - RECBE) is **~1.9 µs.**

Online trigger system

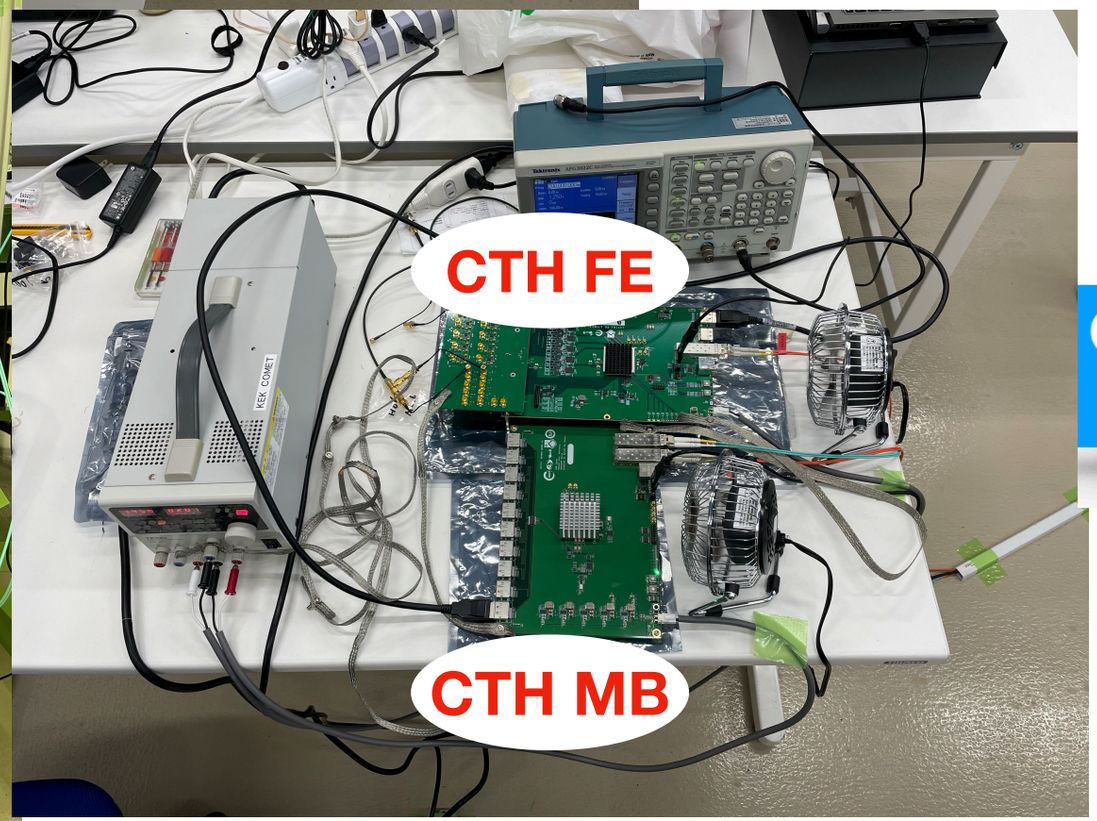


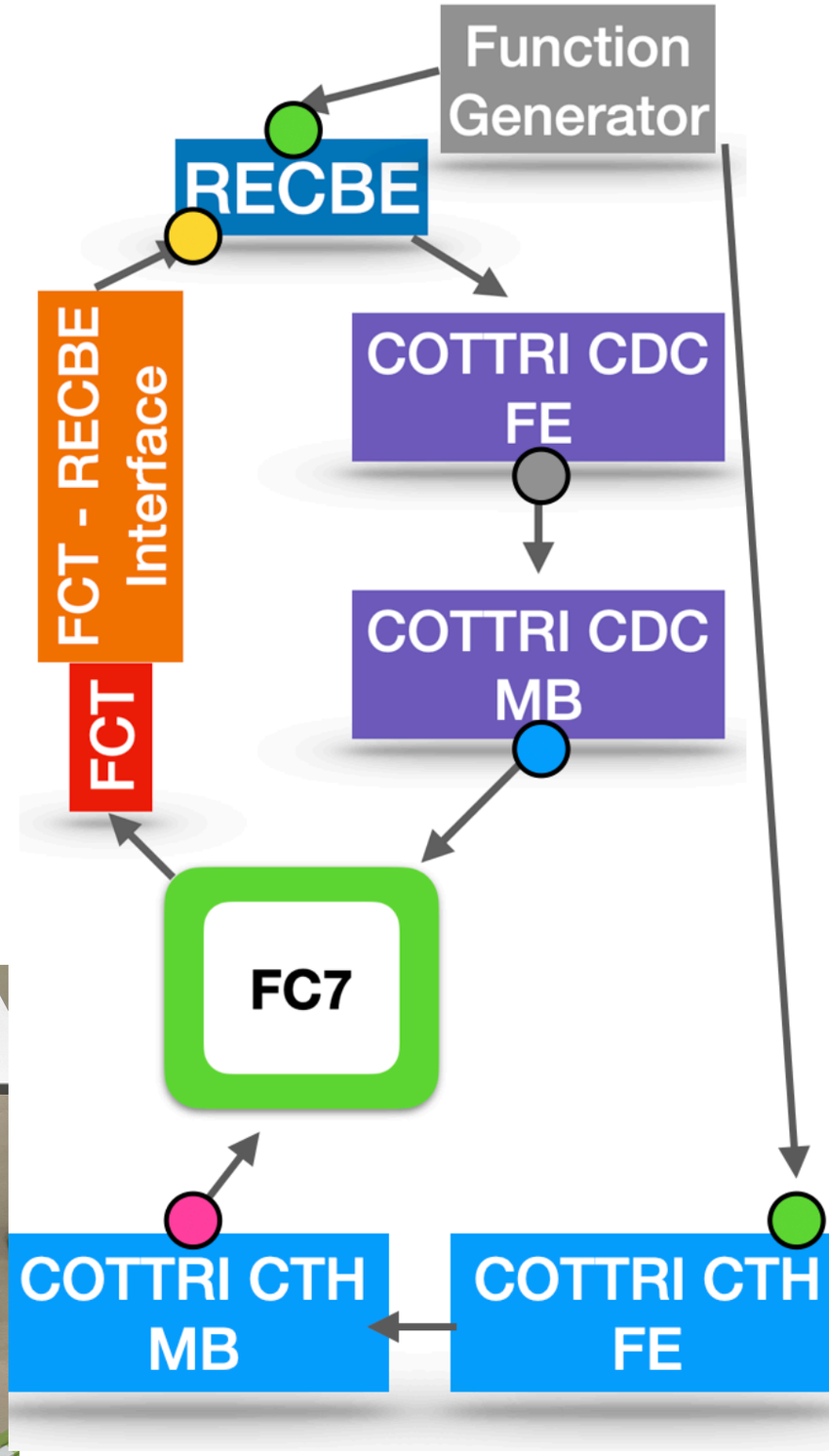
※Yu Nakazawa PhD Thesis Fig2.12

Set up

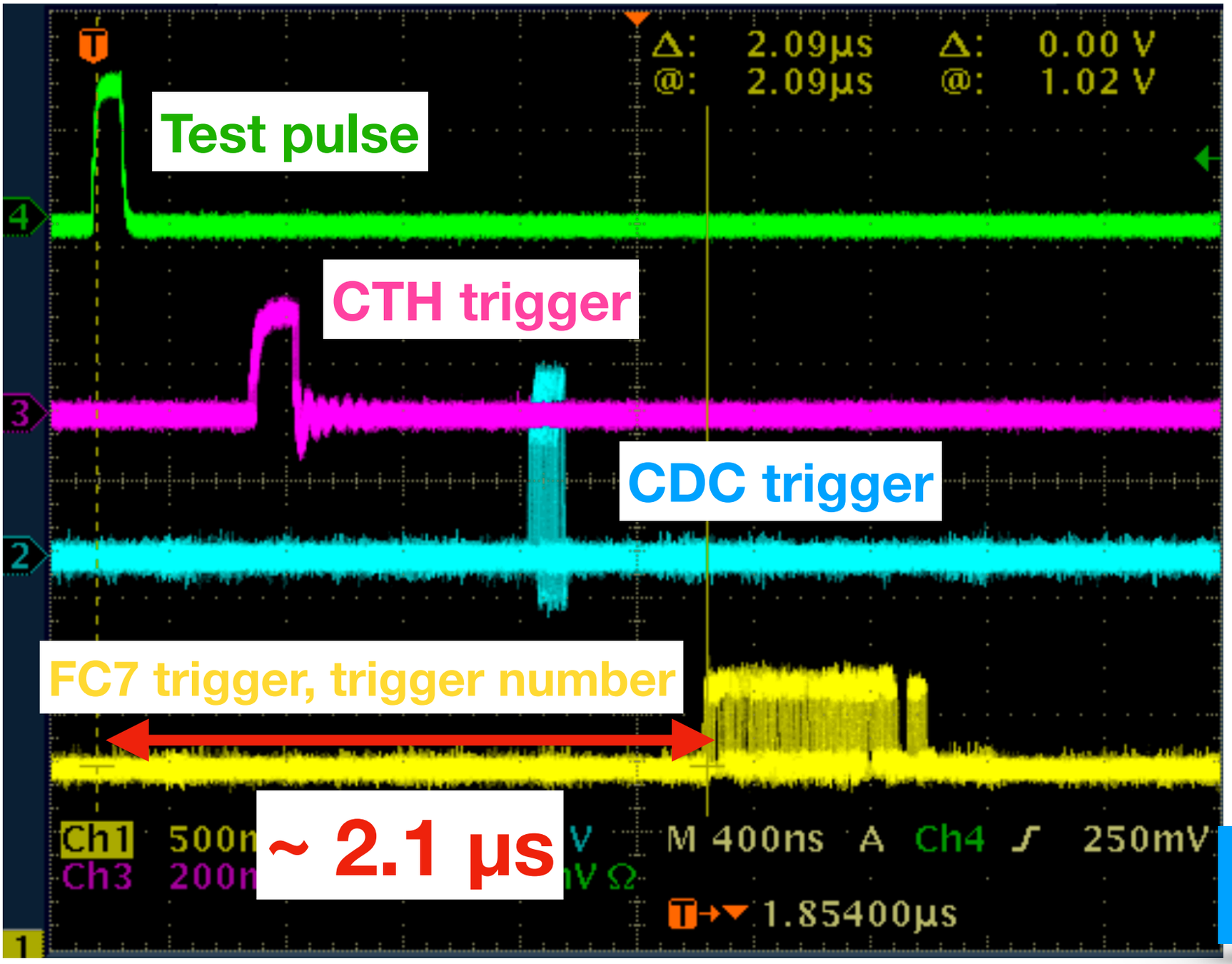

Function generator
Test pulse
Function generator
12 MHz CLK
FCT-RECBE I/F
CDC MB
CDC FE
RECBE

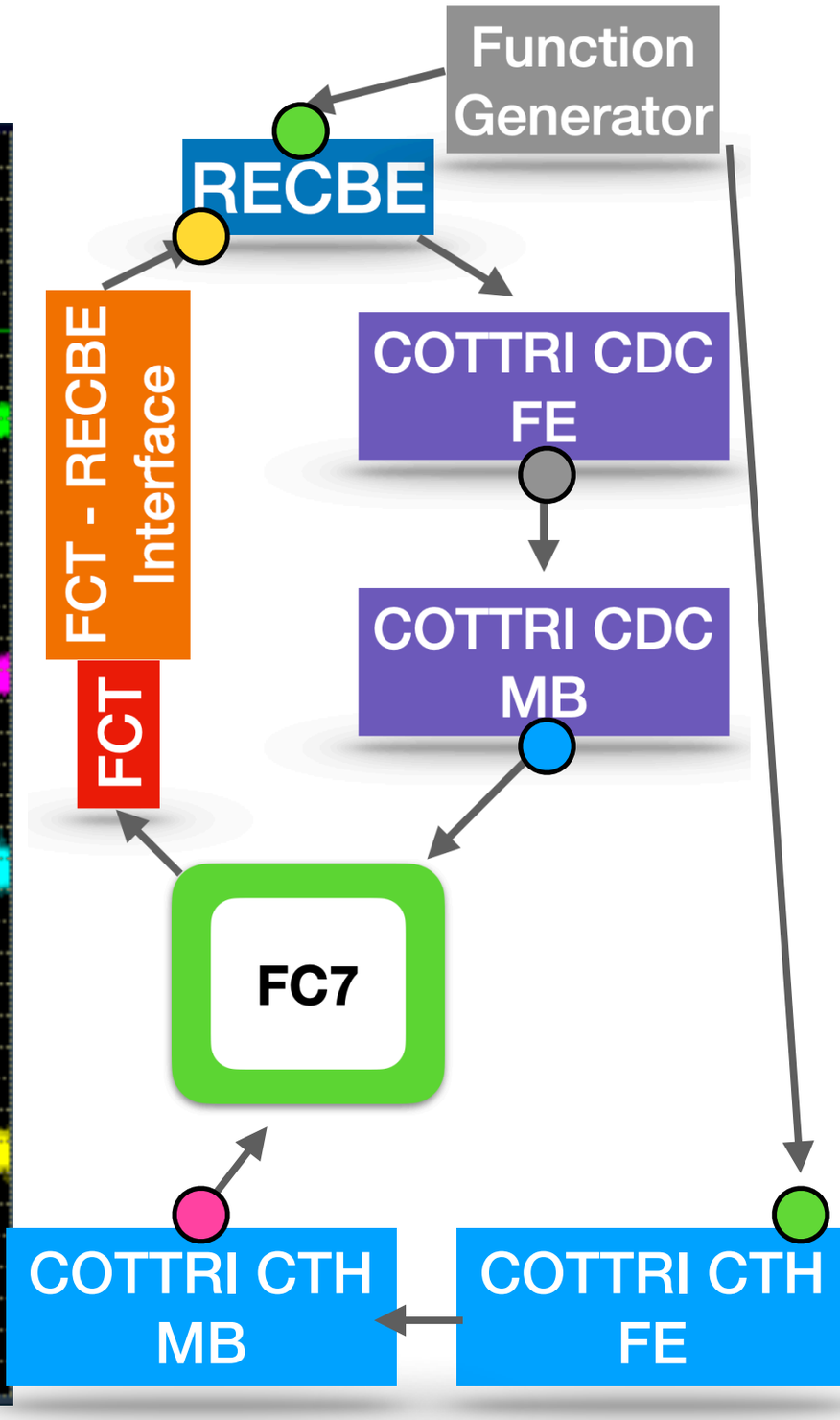

COMET
FC7


CTH FE
CTH MB


Function Generator
RECBE
FCT - RECBE Interface
FCT
COTTRI CDC FE
COTTRI CDC MB
FC7
COTTRI CTH MB
COTTRI CTH FE

Latency measurement



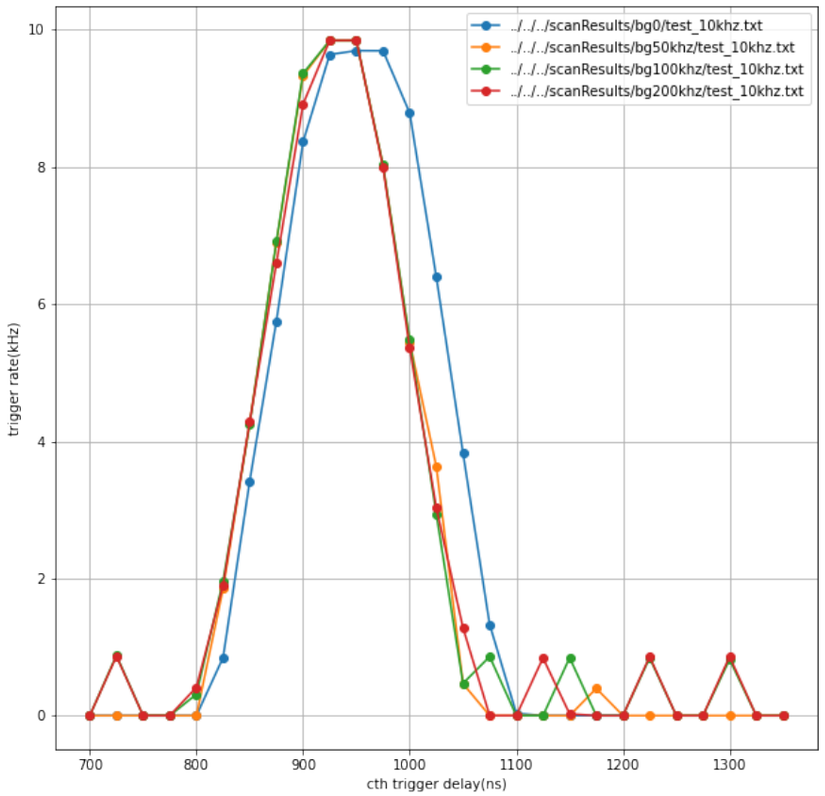


Latency ~ 2.1 µs

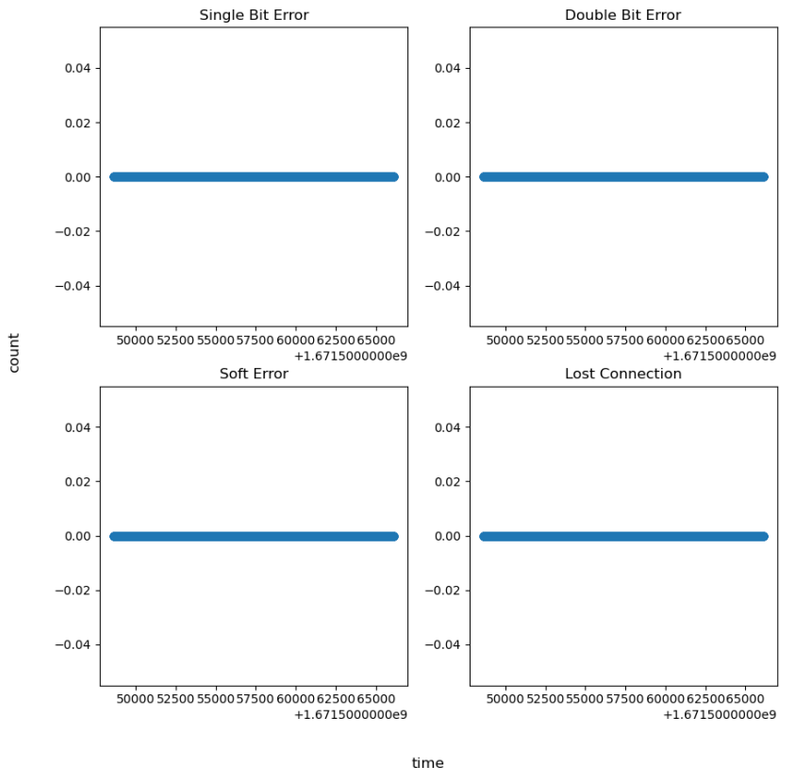
There is no increase in delay due to the coincidence trigger.

Other preliminary results of FC7 coincidence trigger

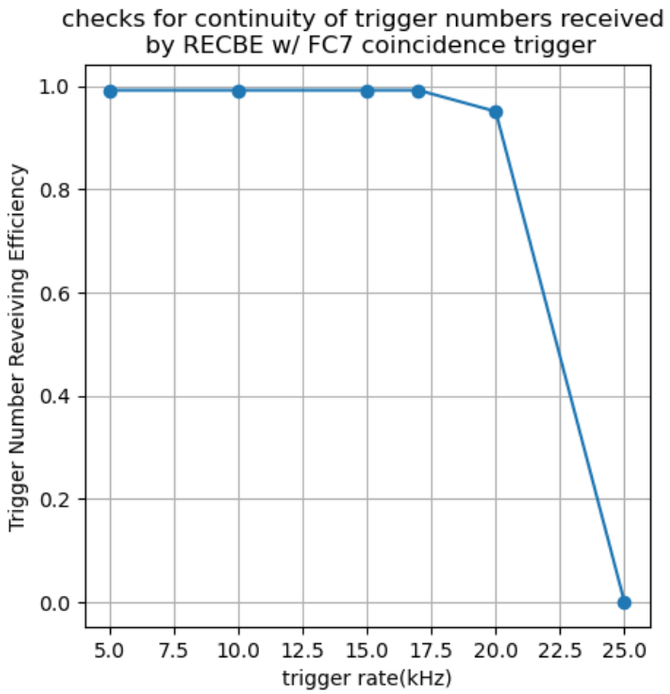
coincidence delay scan

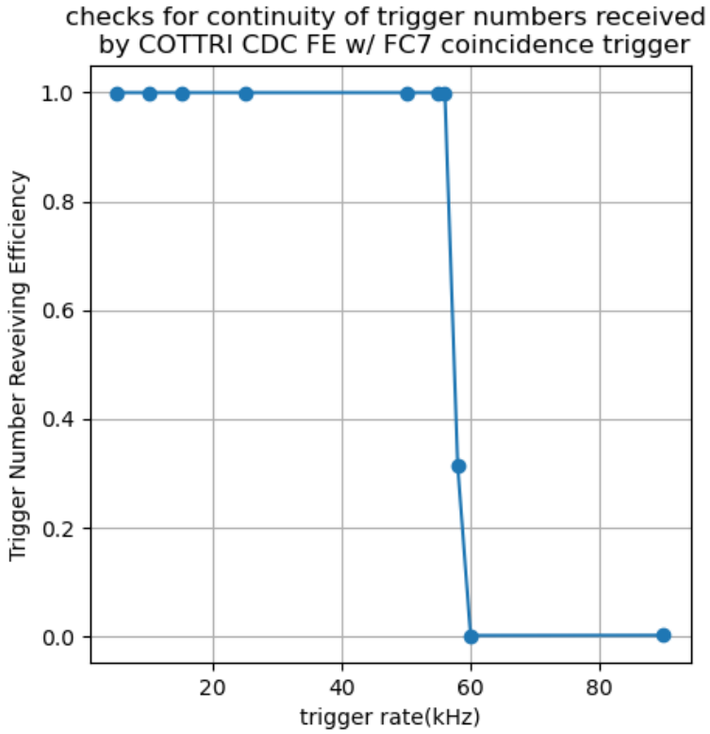


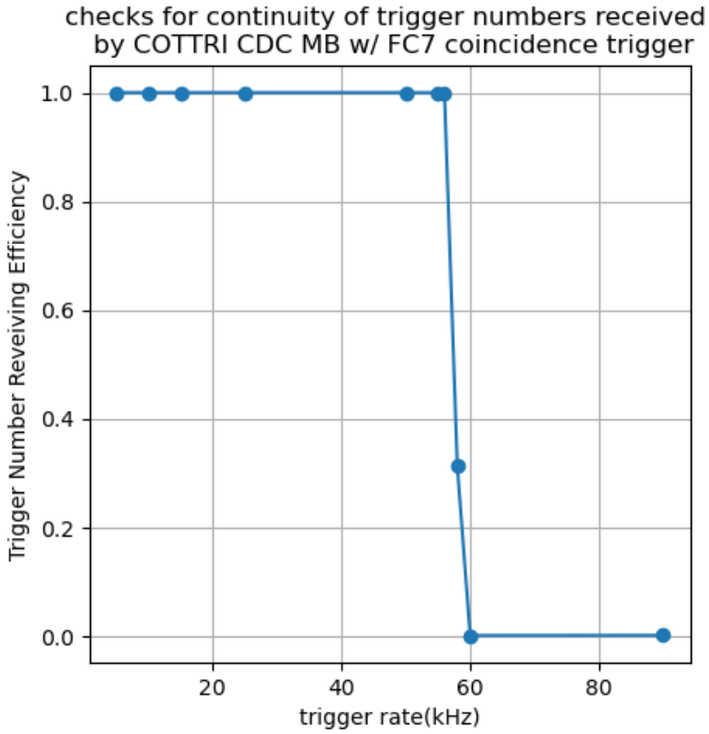
Communication stability check



Trigger number continuity check results







New online event classification algorithm

To improve signal acceptance, increase trigger efficiency, and widen the measurement time window

Measurement time window(ns)	Current system [700,1170]	[500,1170]
Signal acceptance(%)	4.2	7.0

x 1.7

The current trigger system has a trigger rate above 13 kHz for 500 ns start

The current CDC trigger algorithm

= hit classification by ML + event classification by counting signal-like hits

↓

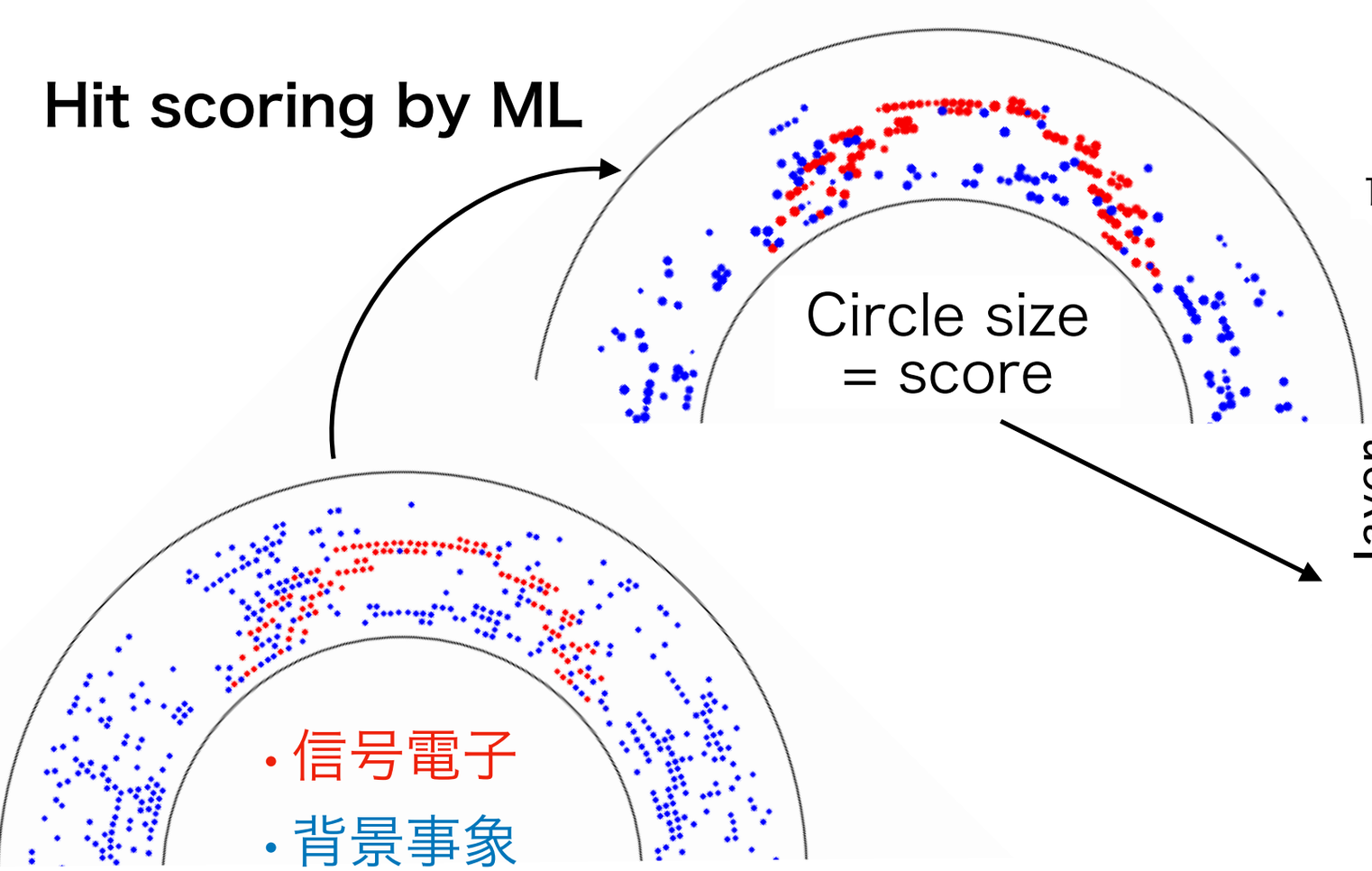
New CDC trigger algorithm under development

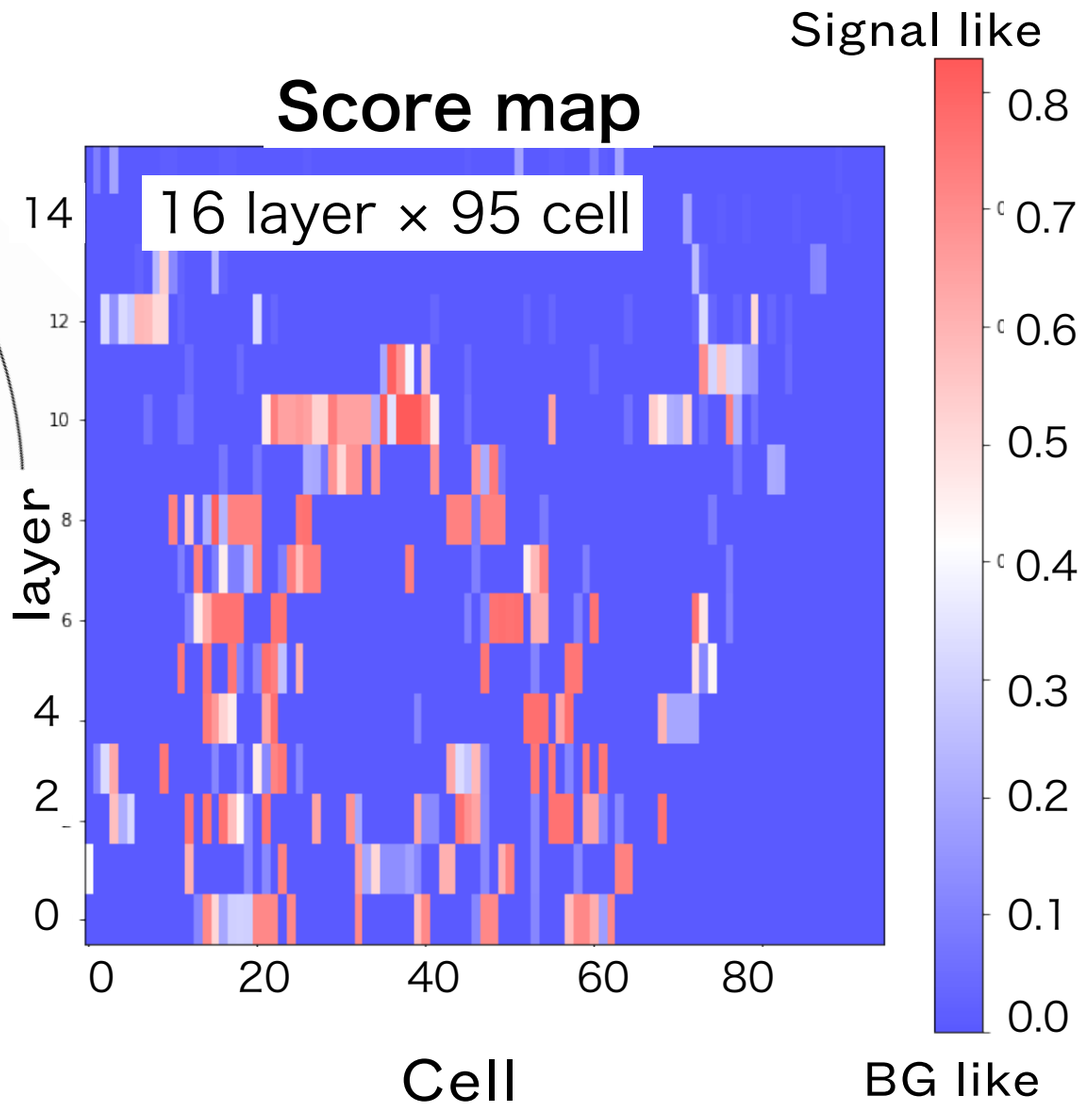
= hit classification by ML + **event classification by Neural Network**

Neural network based event classification

New CDC trigger algorithm under development

= hit classification by ML + event classification by Neural Network

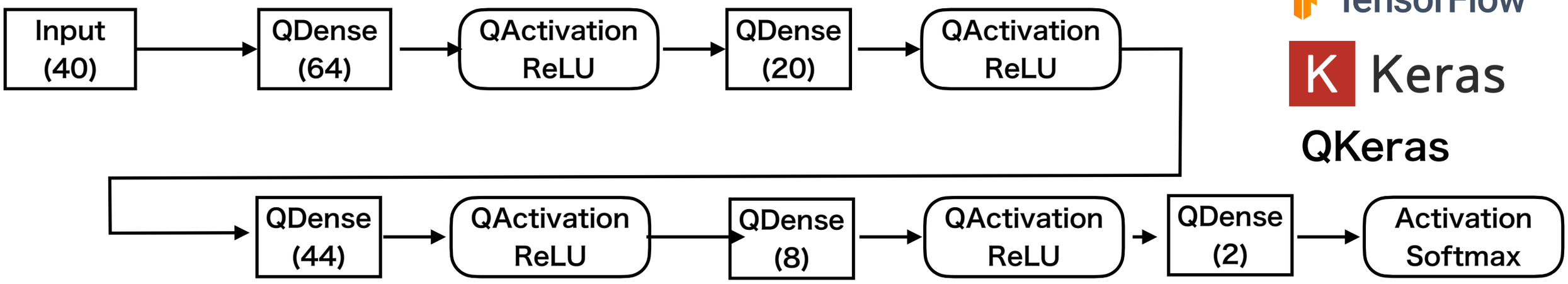




- By using the score map as input to the Neural network, pattern recognition of the trajectory drawn by the signal electrons can be introduced for event classification.

Model construction

Fully connected 5 dense layer Quantized MLP (HPs tuned except for bit width)

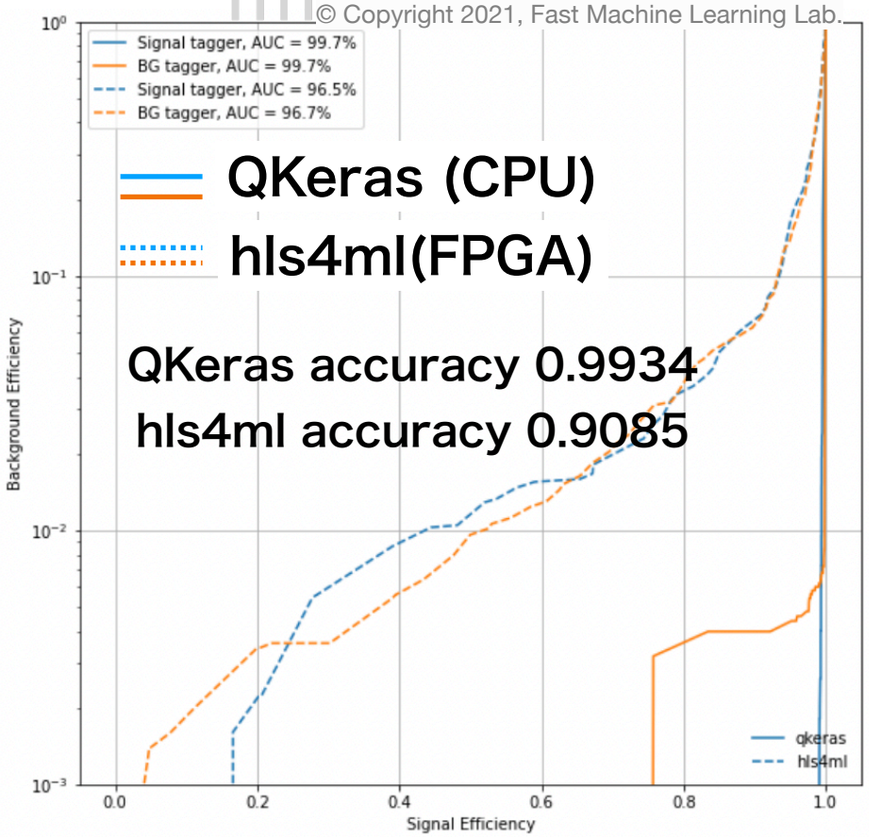


TensorFlow

Keras

QKeras

hls4ml



Convert models into firmware-transformable code(RTL) w/o programing in HDL

https://dx.doi.org/10.1088/1748-0221/13/07/P07027

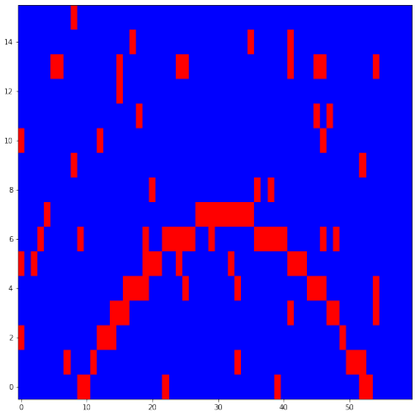
FPGA : AMD Xilinx Kintex-7 xck355t-ffg901-1

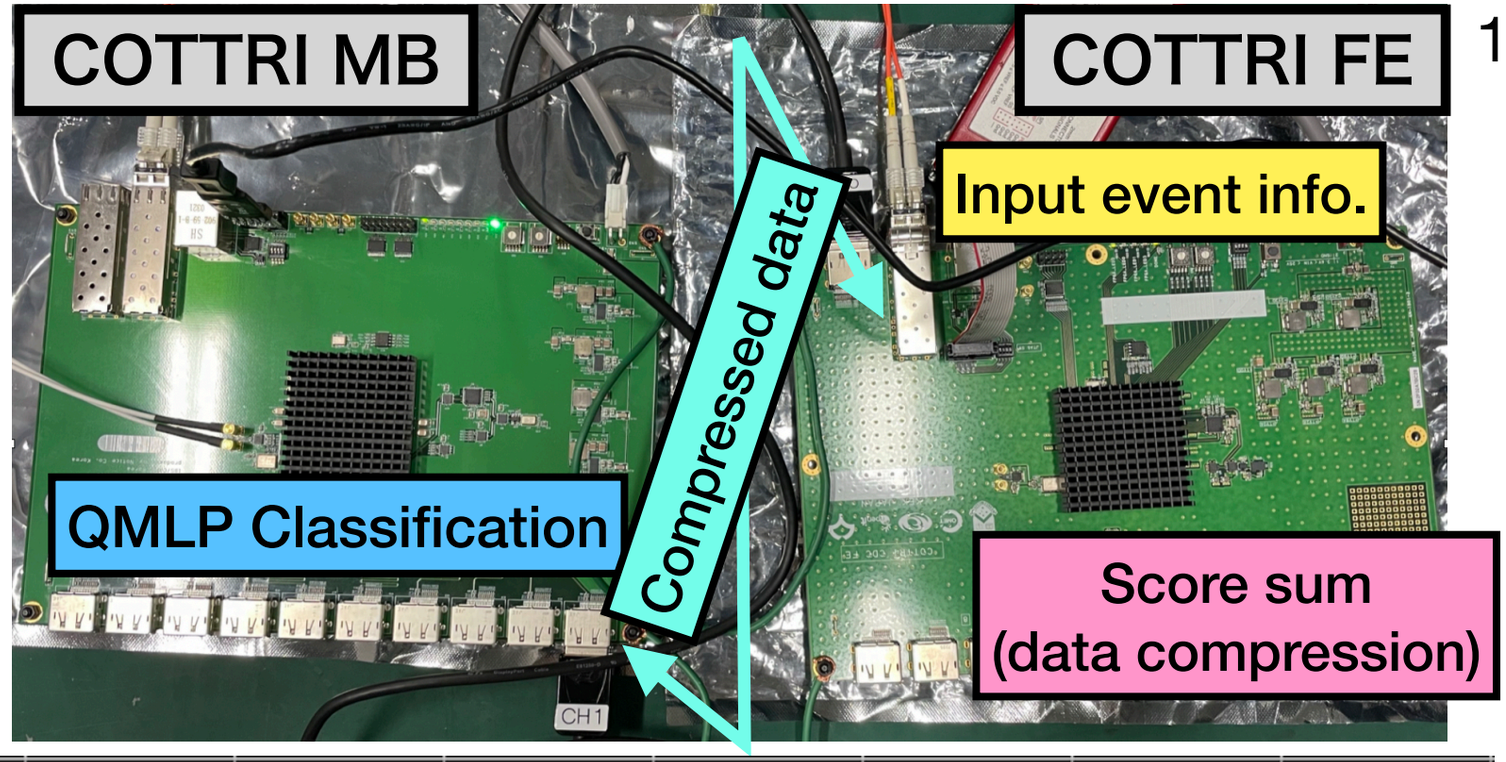
	Usage (%)			
Latency @200MHz	BRAM	DSP	FF	LUT
130 ns	~0	~0	5	32

After high-level synthesis of the C++ file generated by hls4ml with vivado_hls, I generated this QMLP ip in vivado and implemented it into COTTRI MB's firmware.

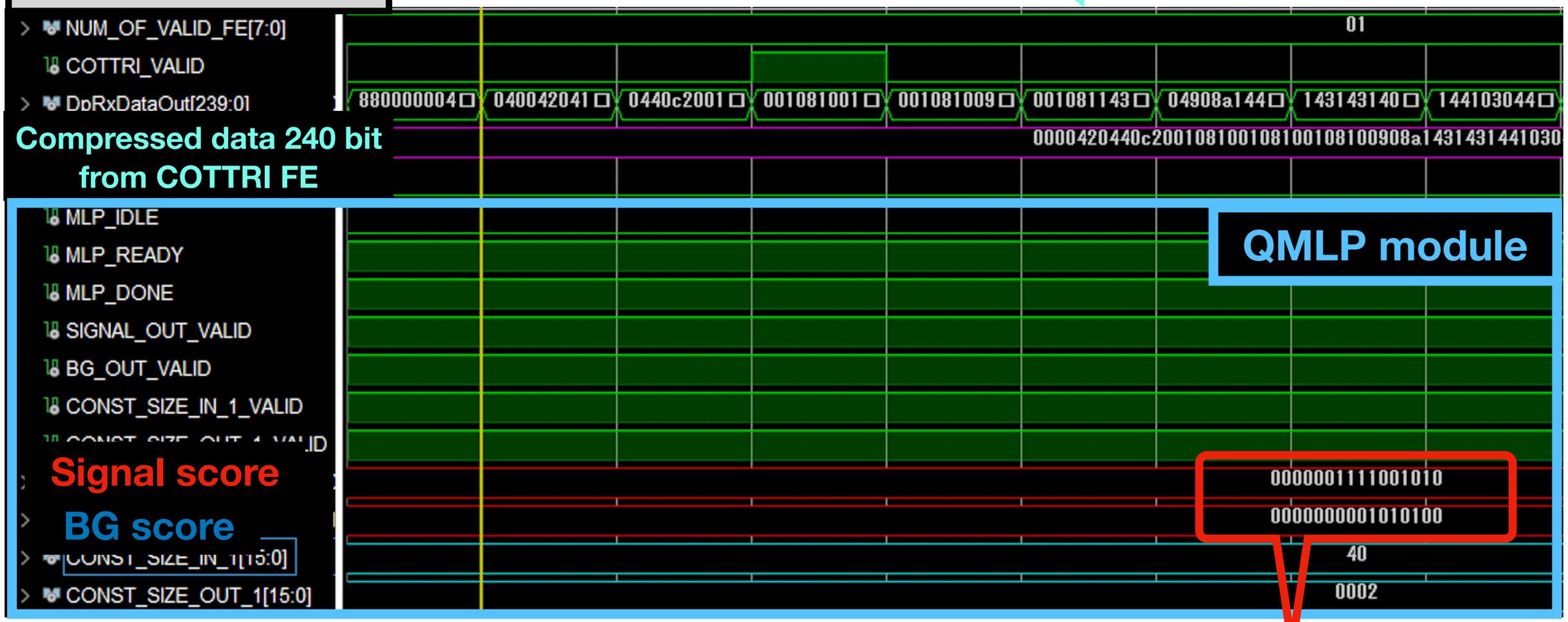
Test

Input event





ILA : COTTRI MB

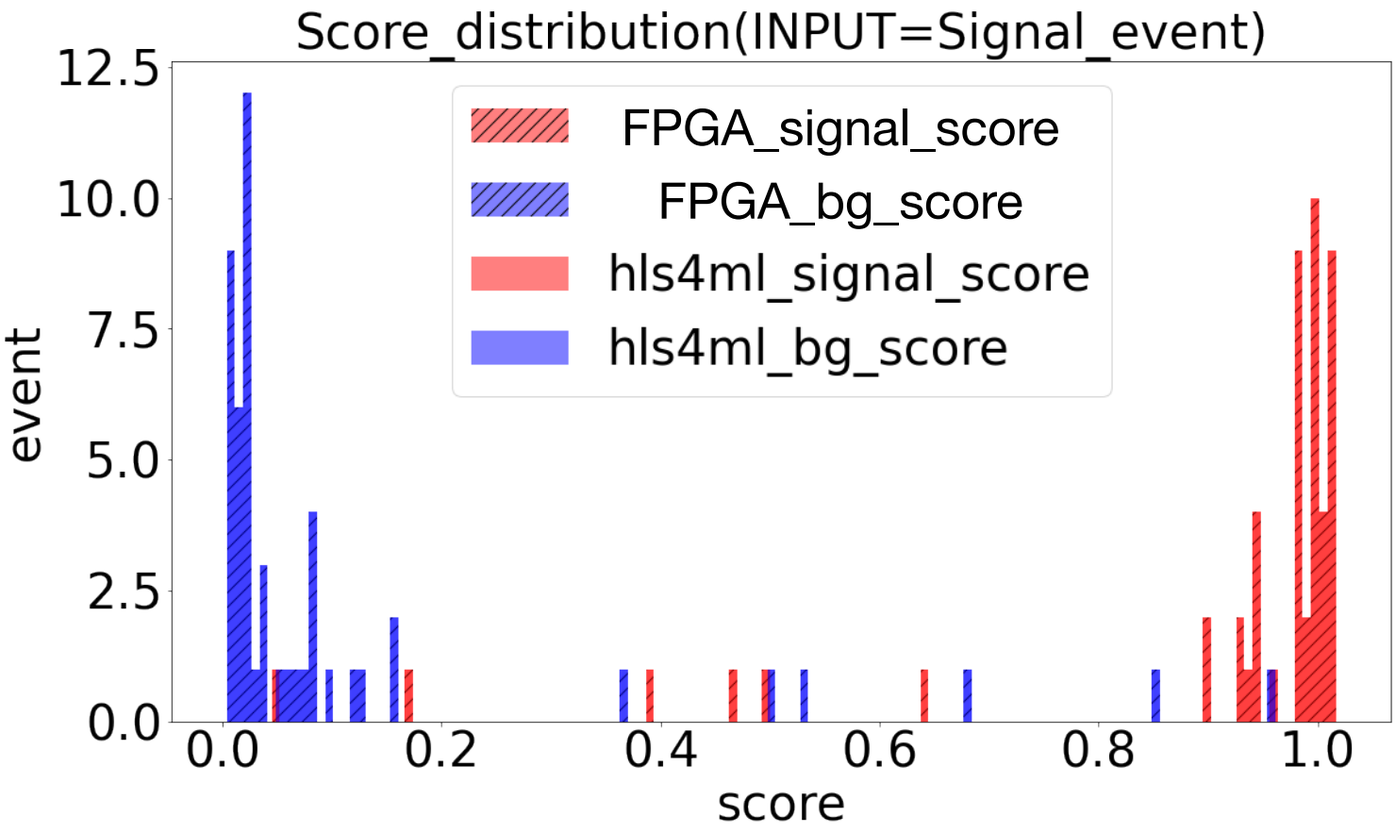


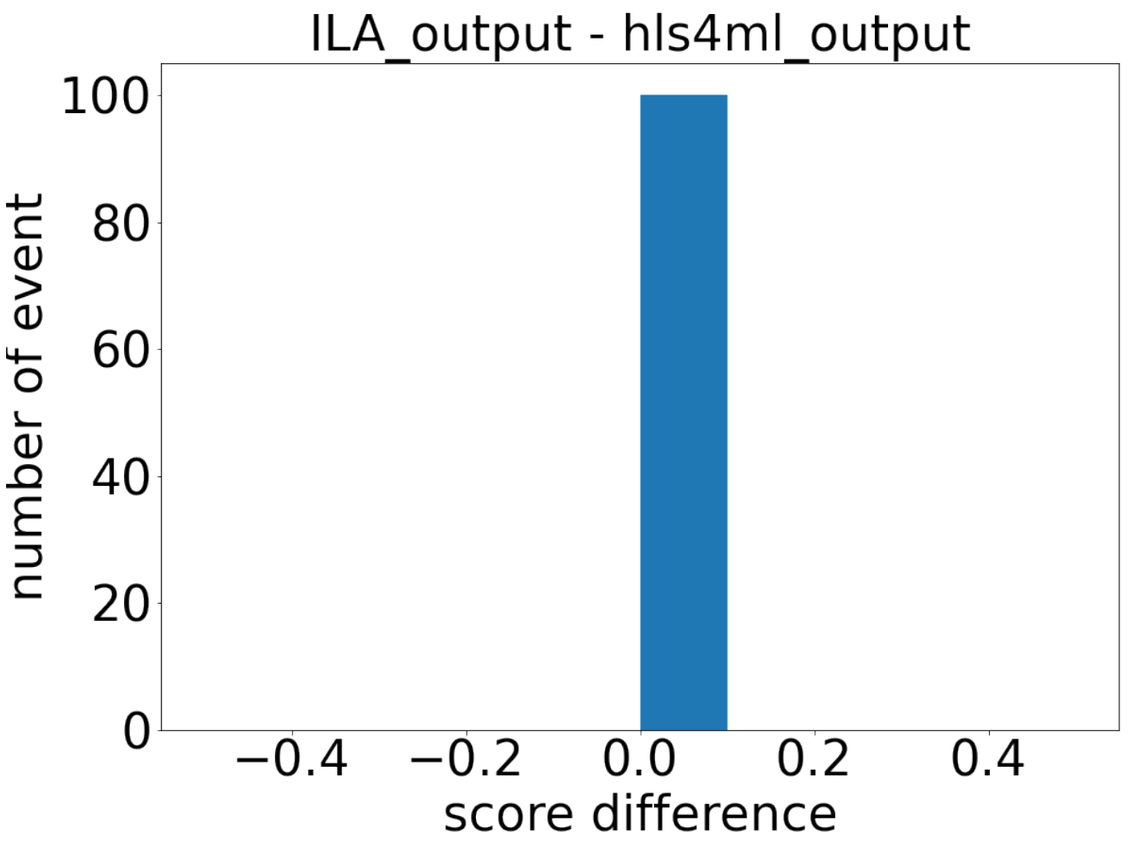
Score as expected 😎

BG score < **Signal score**

0.08 **0.95**

Neural Network test results





software and hardware predicted values are in perfect agreement

Summary

- CDC trigger chain test was conducted.
  - Latency ~ 2 μs
- CyDet trigger chain test was conducted.
  - The FC7 trigger was successfully issued and distributed to whole CyDet trigger system.
  - Latency ~ 2 μs
  - Many tests were carried out. The analysis is ongoing.
- New online event classification study is ongoing.
  - Neural network model that classifies the signal electron event and background event was constructed.
  - The trained model was successfully implemented on FPGA.
  - Software and hardware prediction scores are in perfect agreement.

LV

LV

FG

FG

DP
LV
Optical
Ethernet
JTAG
FTP
Lemo

MTC crate

FC7

12 MHz

MGT link

FCT

RECBE I/F

5 V

Trigger
Signal

MTCA control

CAT7

MGT link

5.5 V
3.8 V
2.0 V
1.5 V

SFP
socket

5 V

SFP
socket

COTTRI CDC ME

SFP
socket

Media
converter

SFP
socket

5 V

SFP
socket

COTTRI CDC FE

SFP
socket

Media
converter

adapter

SFP
socket

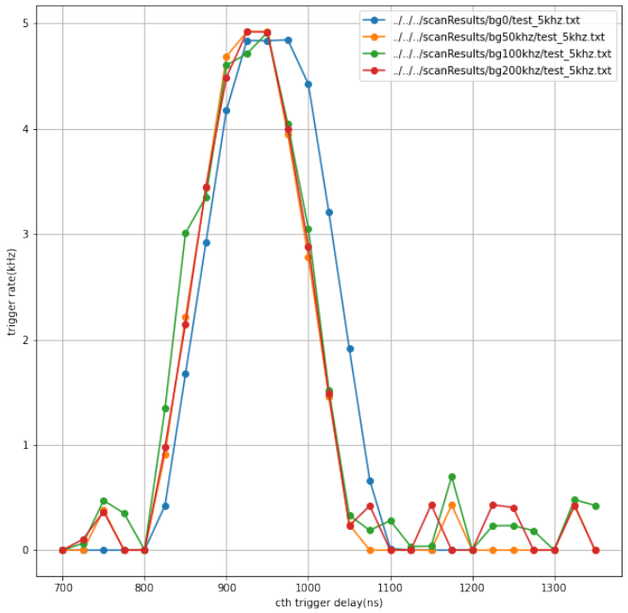
RECBE

SFP
socket

Media
converter

Ether hub
+ PC

FC7PC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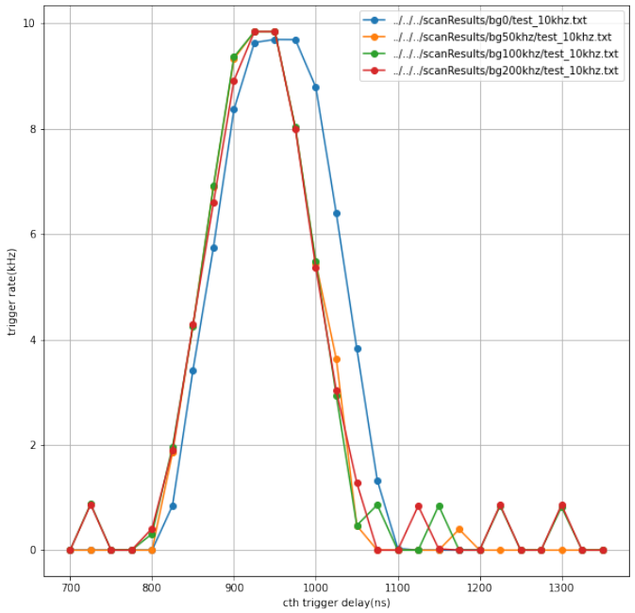
trigger rate(kHz)
cth trigger delay(ns)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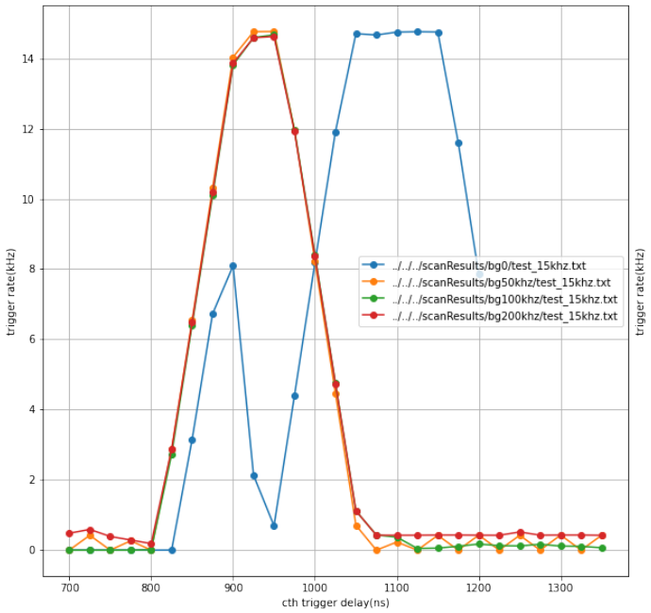
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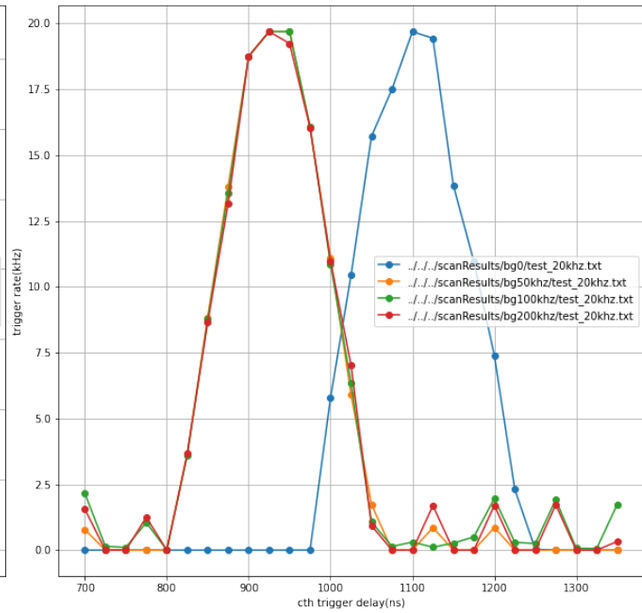
trigger rate(kHz)
cth trigger delay(ns)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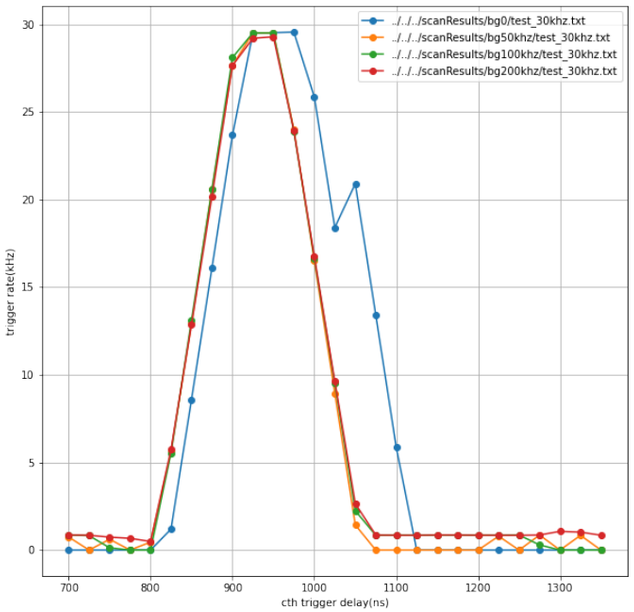
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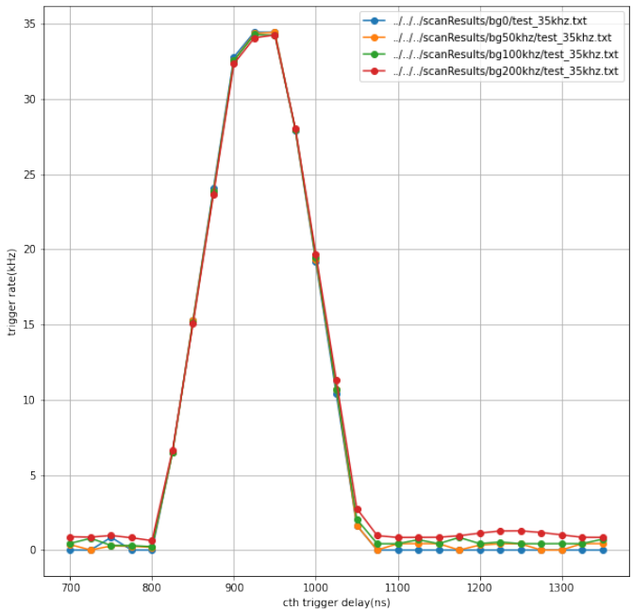
cth trigger delay(ns)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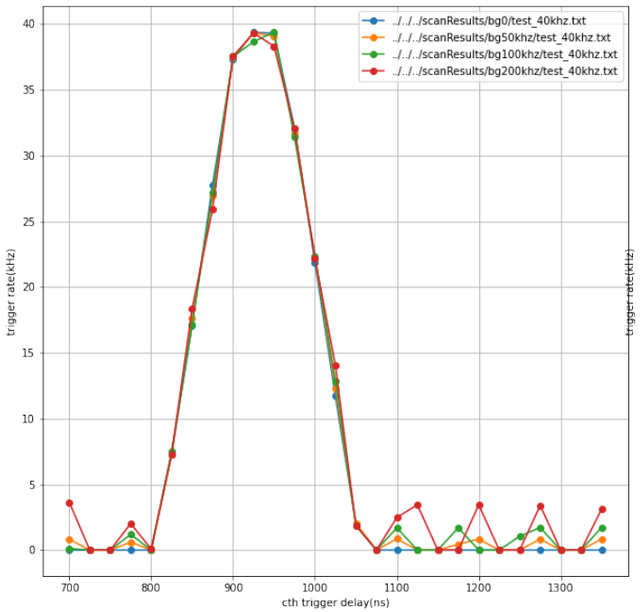
trigger rate(kHz)
cth trigger delay(ns)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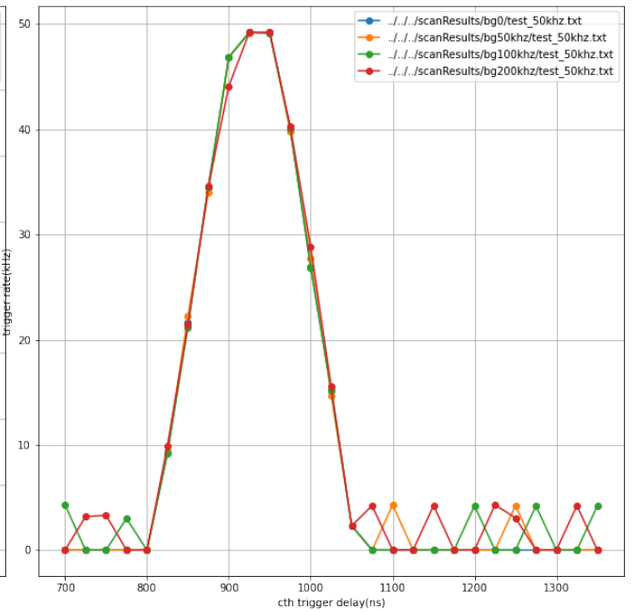
trigger rate(kHz)
cth trigger delay(ns)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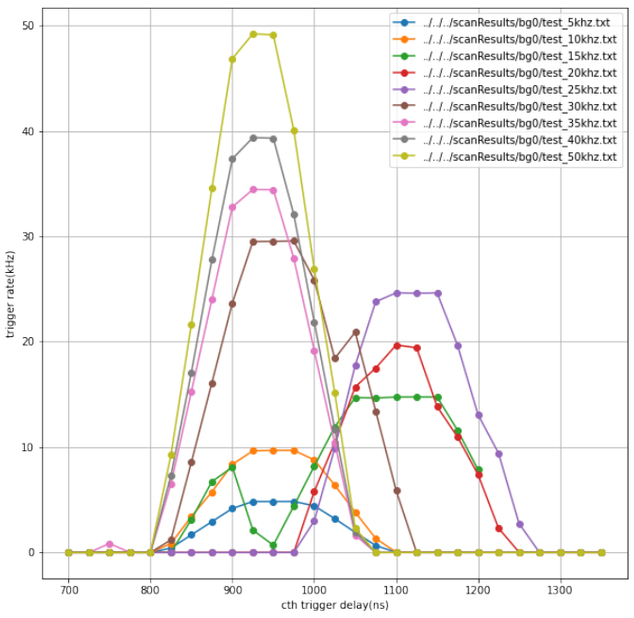
trigger rate(kHz)
cth trigger delay(ns)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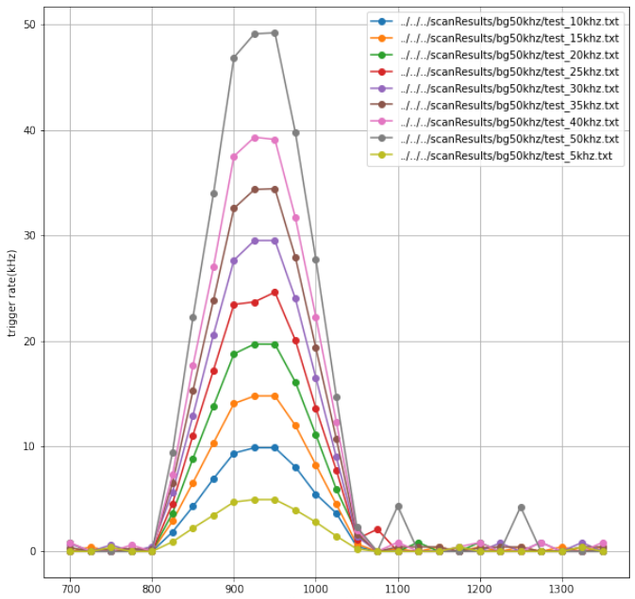
trigger rate(kHz)
cth trigger delay(ns)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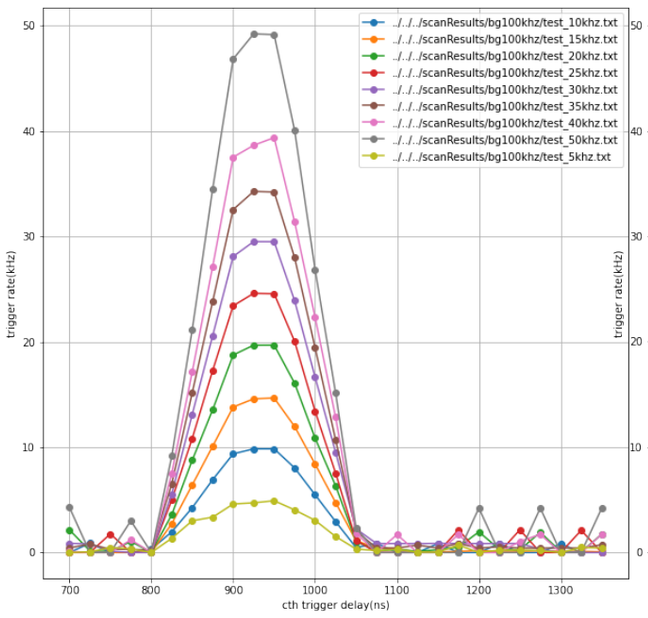
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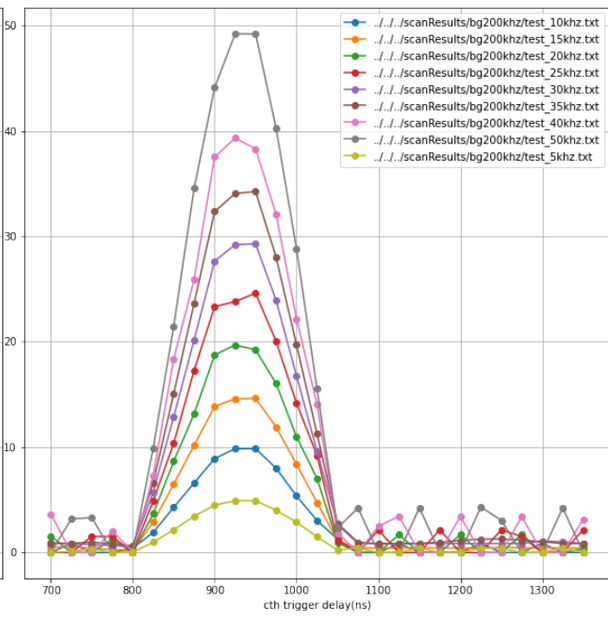
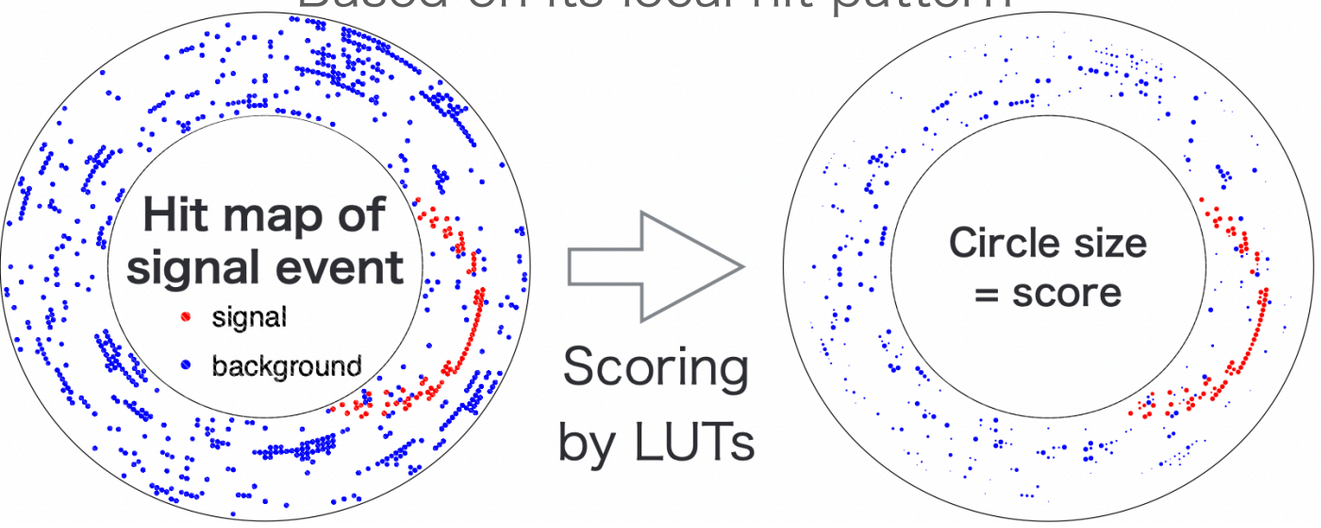
../../../scanResults/bg100khz/test_25khz.txt
../../../scanResults/bg100khz/test_30khz.txt
../../../scanResults/bg100khz/test_35khz.txt
../../../scanResults/bg100khz/test_40khz.txt
../../../scanResults/bg100khz/test_50khz.txt
../../../scanResults/bg100khz/test_5khz.txt
trigger rate(kHz)
cth trigger delay(ns)


../../../scanResults/bg200khz/test_10khz.txt
../../../scanResults/bg200khz/test_15khz.txt
../../../scanResults/bg200khz/test_20khz.txt
../../../scanResults/bg200khz/test_25khz.txt
../../../scanResults/bg200khz/test_30khz.txt
../../../scanResults/bg200khz/test_35khz.txt
../../../scanResults/bg200khz/test_40khz.txt
../../../scanResults/bg200khz/test_50khz.txt
../../../scanResults/bg200khz/test_5khz.txt
trigger rate(kHz)
cth trigger delay(ns)

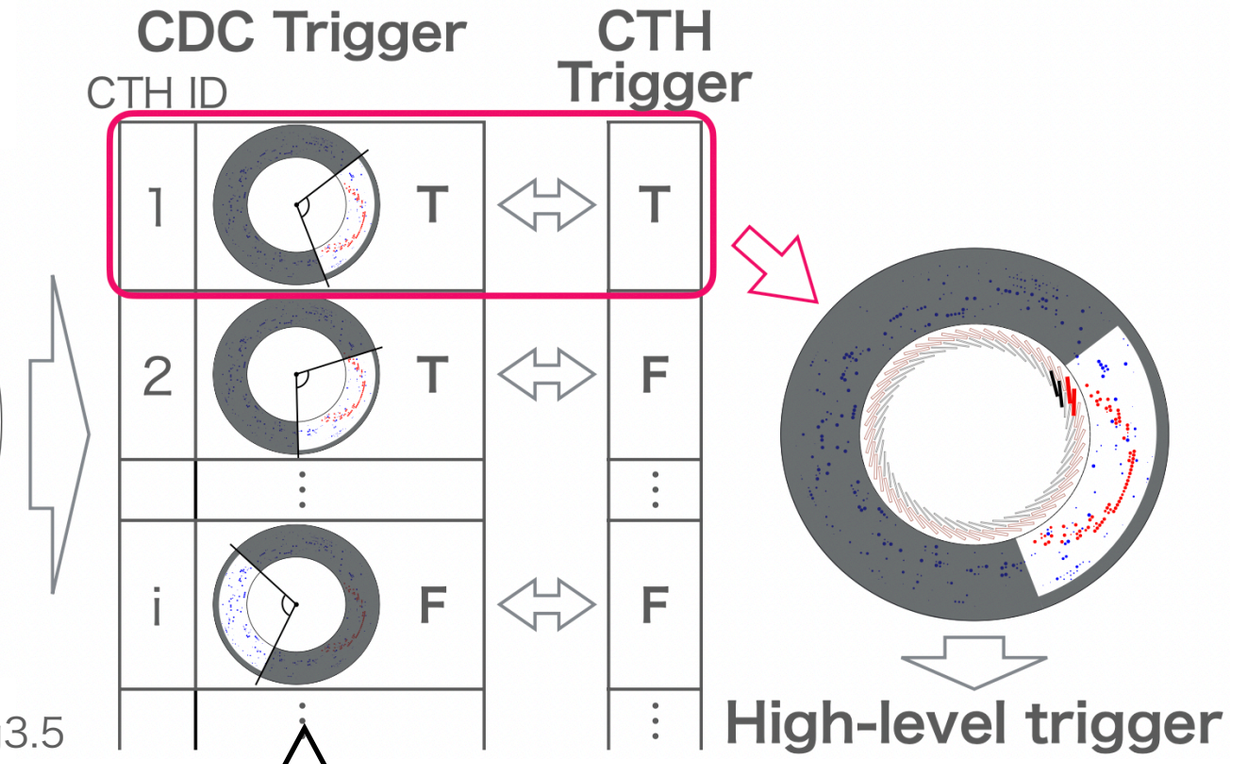
Trigger algorithm

Hit classification

GBDT gives each wire hit a score
Based on its local hit pattern



Event classification



Yu nakazawa PhD thesis Fig3.5

The current CDC trigger algorithm

1. Set the CDC active section for each segment of CTH
2. Within each active section, count hits that exceed the score threshold
3. CDC trigger is issued when the count exceeds the threshold.

New CDC trigger algorithm under development

1. Set the CDC active section for each segment of CTH

2'. Execute Neural Network inference w/ score information of each active section as inputs

3'. CDC Trigger is issued based on Neural Network classification.

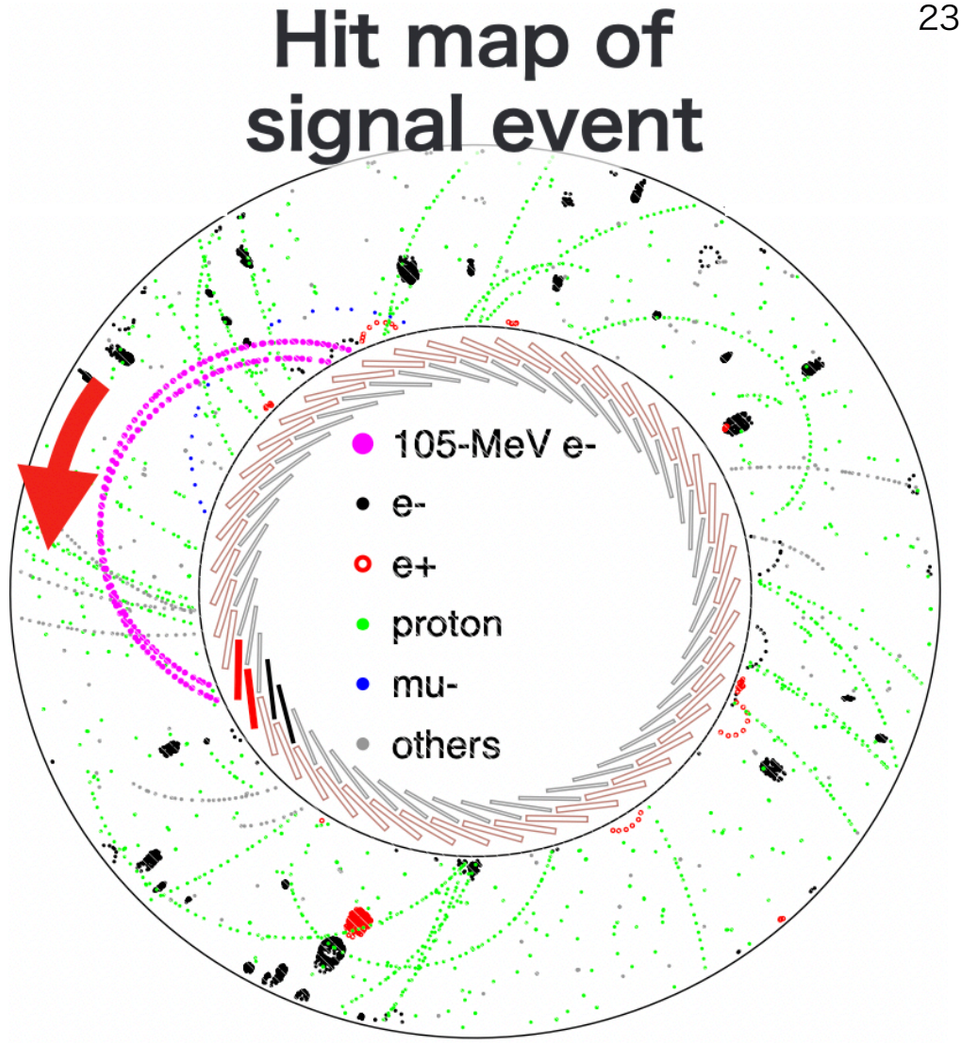
Signal and BG hits

Signal-hit characteristics

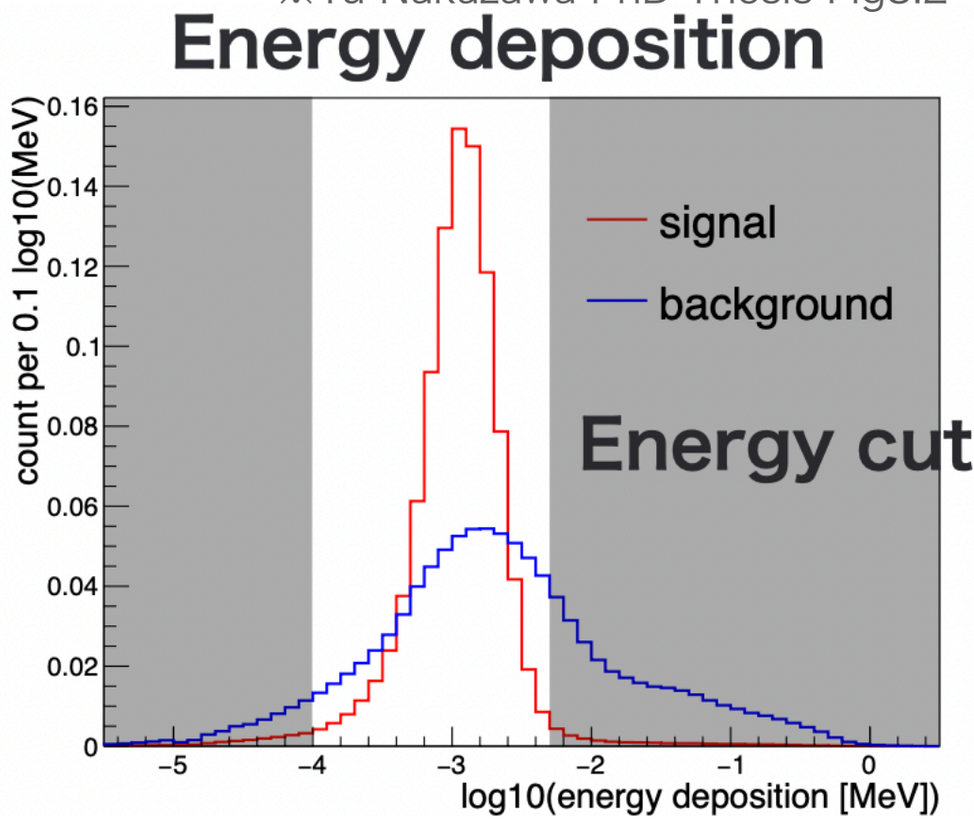
- Contained helical tracks
- Single hit in the same wire
- MIP-level energy loss

Background-hit characteristics

- Low energy electrons
  - Interaction of gamma rays at the CDC walls
  - Helical trajectory contained in the same cell
  - **Multi hits in the same wire**
- Protons (from muon nuclear capture)
  - Momentum higher than 100MeV/c
  - **Large energy loss**
  - ~40 protons/beam-pulse



※Yu Nakazawa PhD Thesis Fig3.2



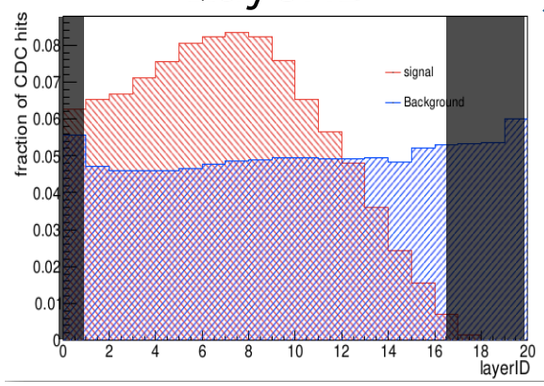
Hit classification

*GBDT = Gradient Boosted Decision Tree

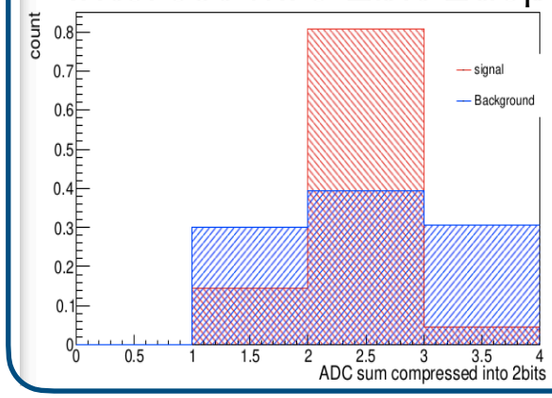
- Machine learning algorithm (GBDT*) to score hit information for each wire based on energy loss and local patterns

GBDT input features

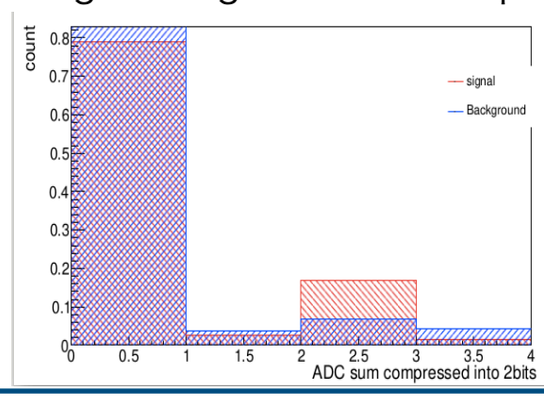
LayerID



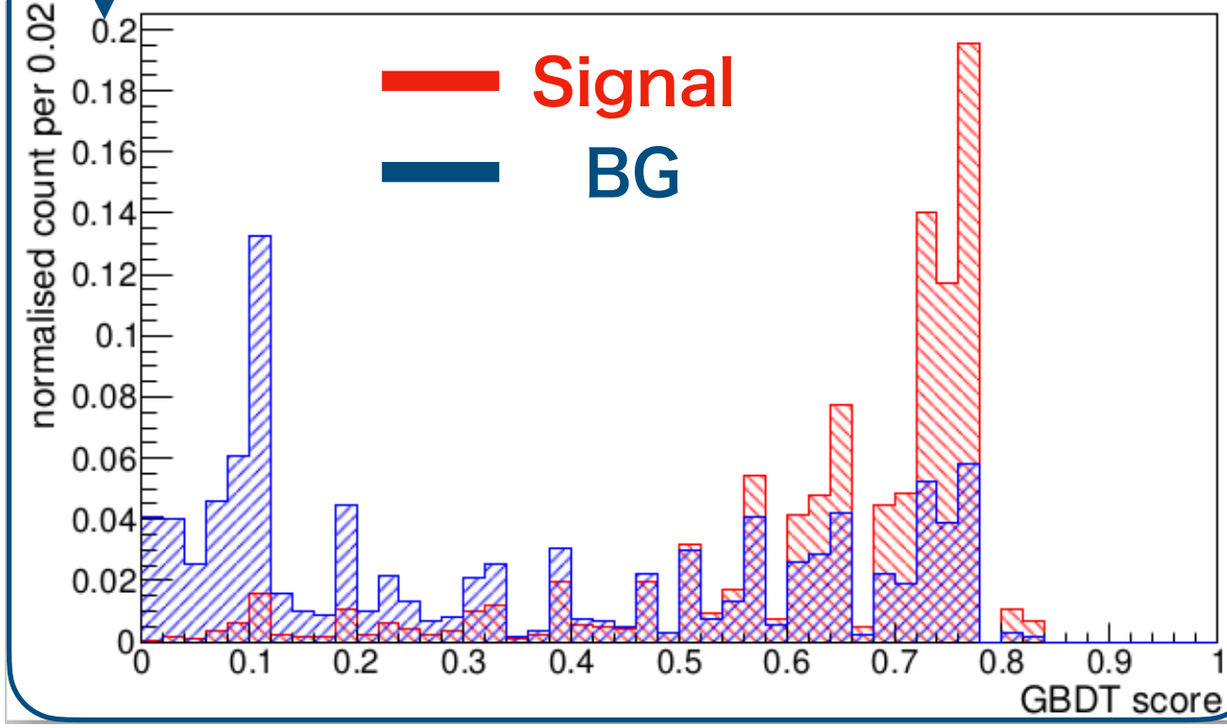
Interest wire 2bit Edep



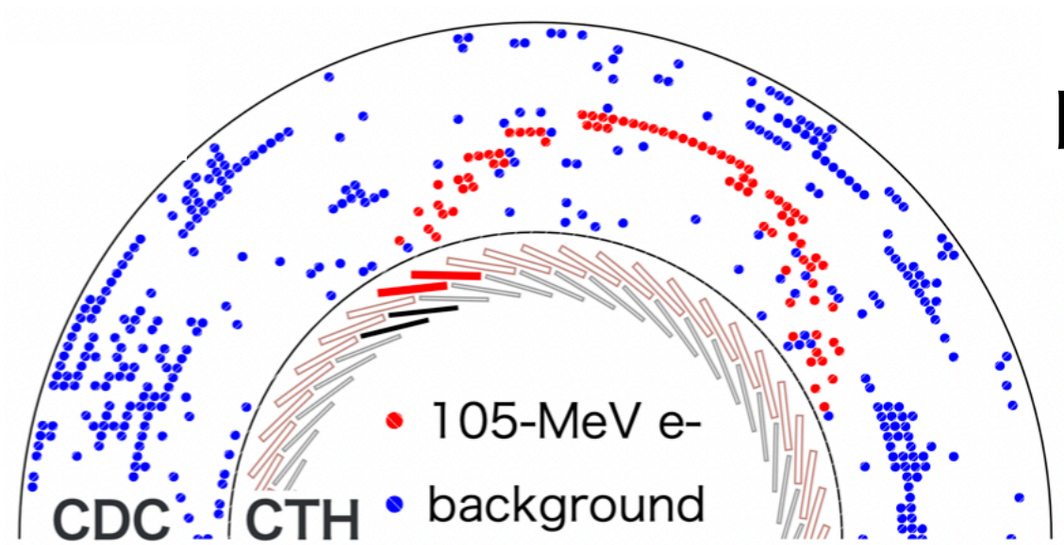
Neighboring wire 2bit Edep



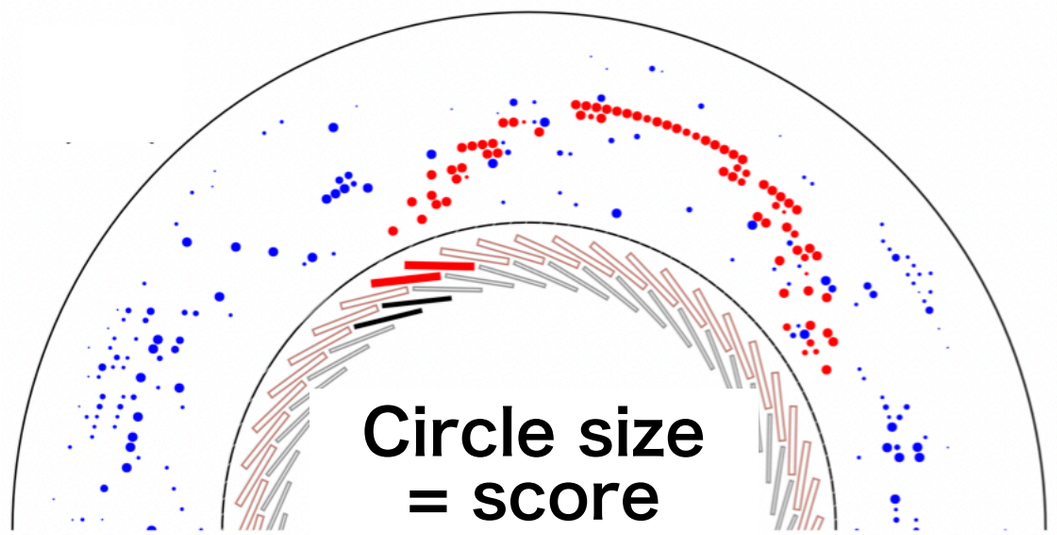
GBDT output score distribution



Hit map of signal event



Scoring By GBDT

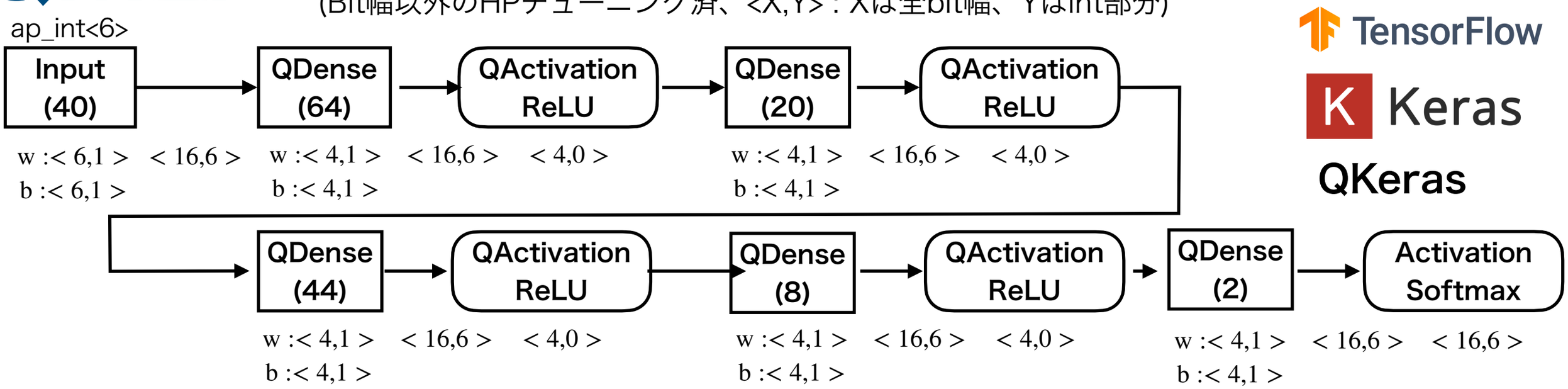


https://doi.org/10.1109/tns.2021.3084624

	CDC config	BG hit 占有率	ワイヤーヒット score情報	Active section
現実	20 layer x ~250 cell	~20 %	6 bit	~1500 ch
本スタディ	18 layer x 180 cell	5%	1 bit	960 ch

QMLP

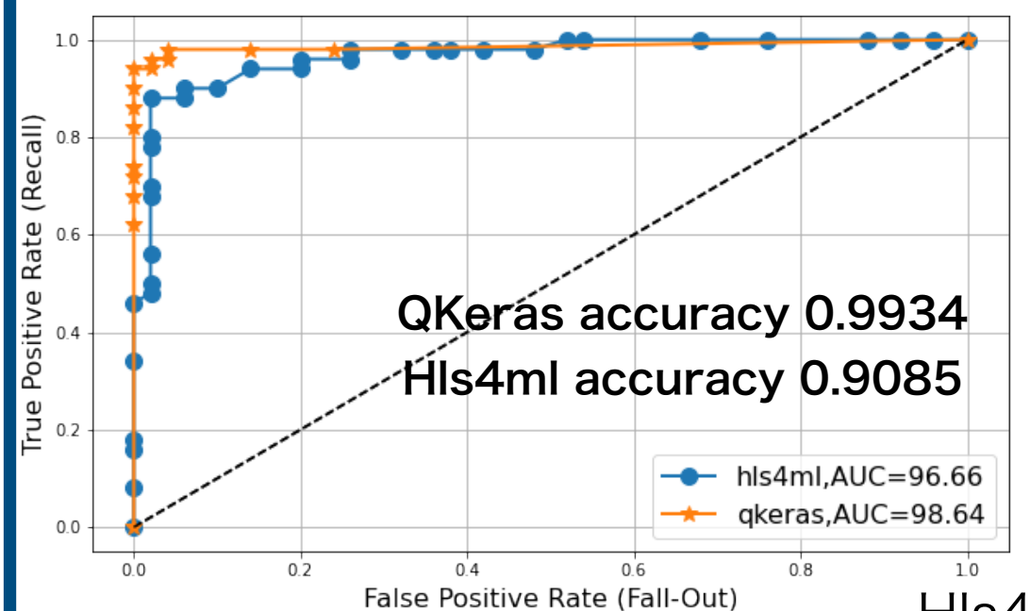
(Bit幅以外のHPチューニング済、<X,Y> : Xは全bit幅、Yはint部分)



モデルをハードウェア記述言語によるプログラミングなしにファームウェア変換可能なコード(RTL)に変換

https://dx.doi.org/10.1088/1748-0221/13/07/P07027

FPGA : AMD Xilinx Kintex-7 xck355t-ffg901-1



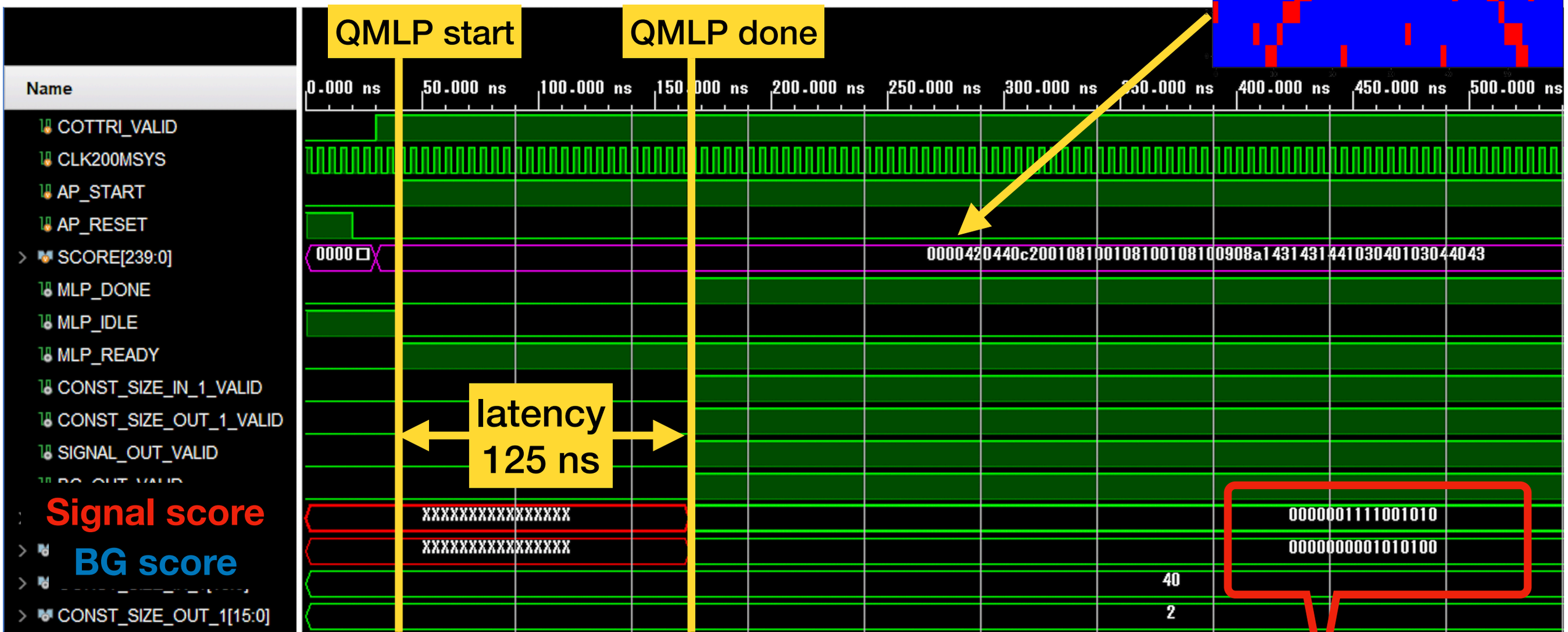
	Usage (%)			
Latency @200MHz	BRAM	DSP	FF	LUT
130 ns	~0	~0	5	32

Hls4mlが生成したC++ファイルをVivado_hlsで高位合成した後、vivadoでこのQMLPのipを生成し、COTTRI MBのFWに組み込んだ

QMLP module simulation

Xilinx vivado simulationによりQMLP moduleのlatencyと出力を確認

信号イベント情報を入力した時のwaveform

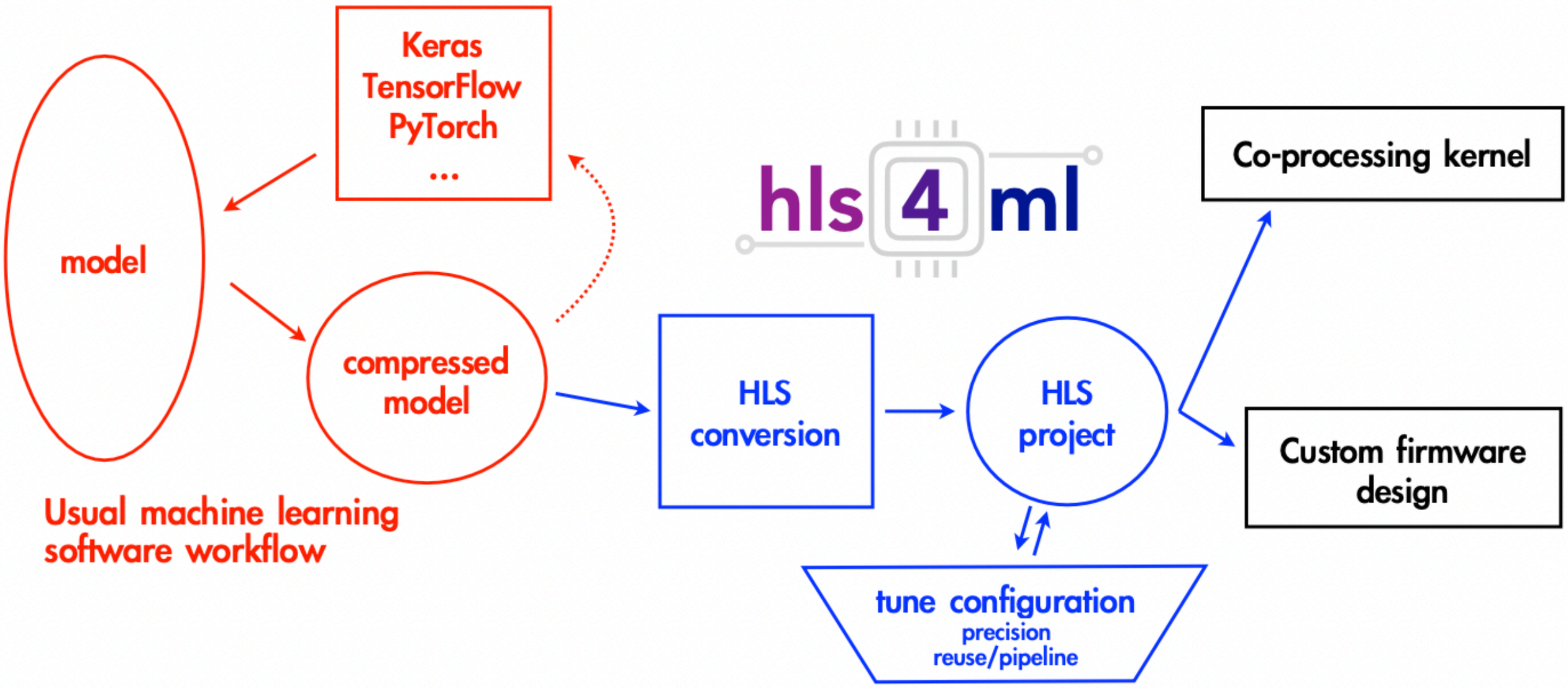


latency, score出力予想通り😎

BG score < **Signal score**

0.08 **0.95**

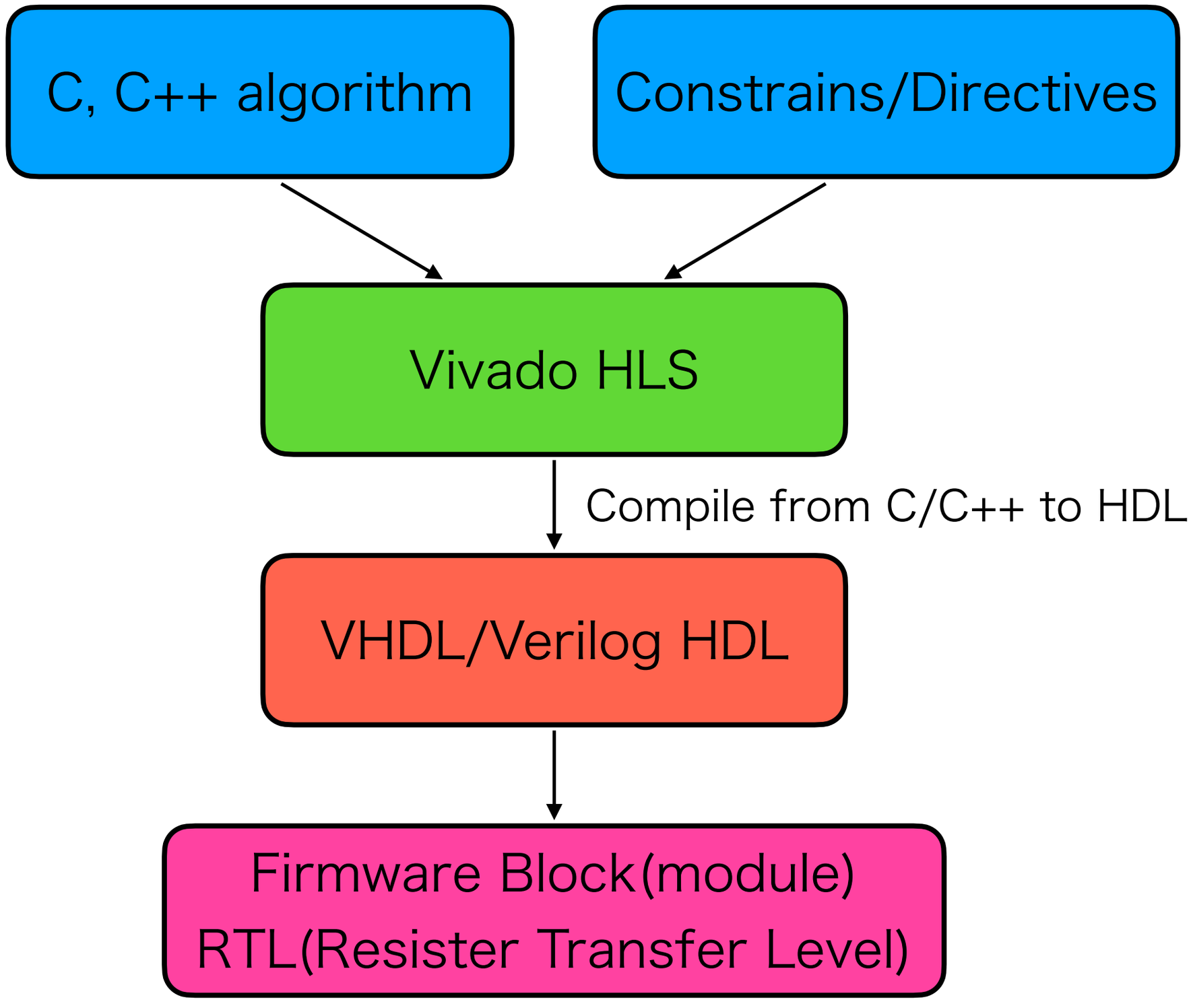
High level synthesis for machine learning



Fast inference of deep neural networks in FPGAs for particle physics Fig1.

https://dx.doi.org/10.1088/1748-0221/13/07/P07027

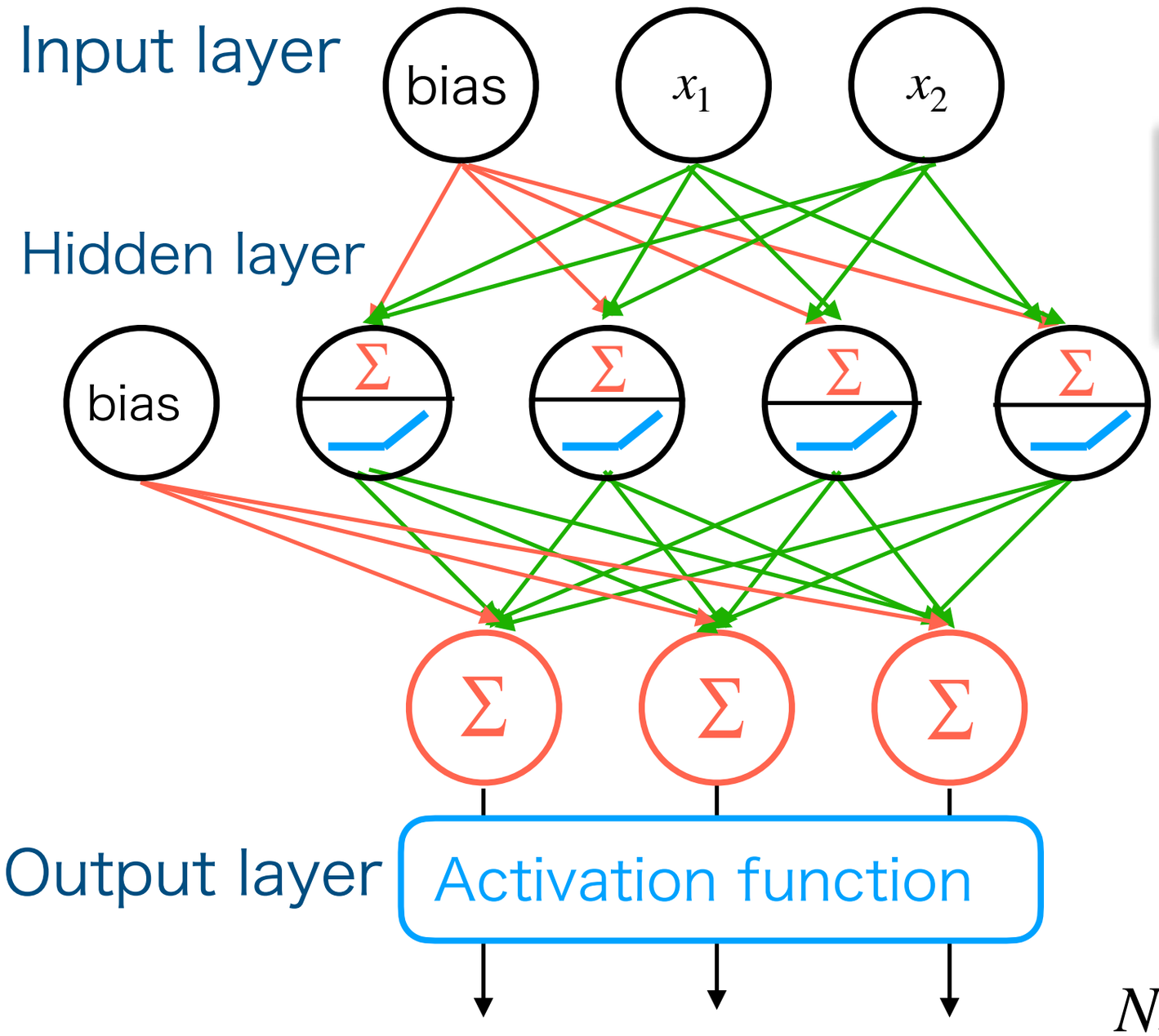
FPGA programing Flow



Neural Network on FPGA

Correspondence between Neural Network operation and FPGA resources

Ex)One-hidden-layer



Vector of neuron output values at each layer

Matrix of weight

$$\mathbf{x}_m = g_m\left(\mathbf{W}_{m,m-1}\mathbf{x}_{m-1} + \mathbf{b}_m\right)$$

Activation Function
- Precomputed and Stored in BRAMs

Multiplication
- DSPs

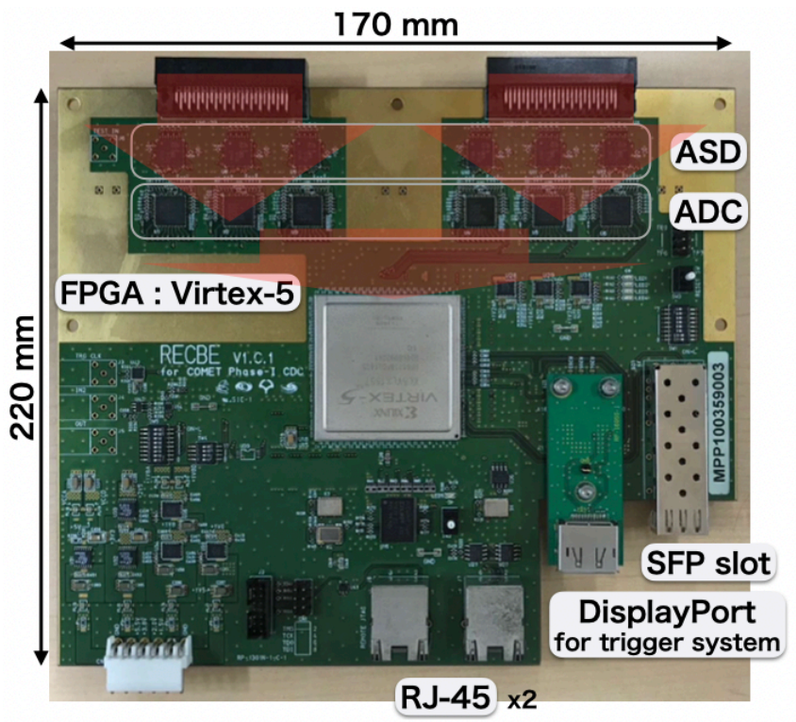
Addition
Logic cells

$$N_{multiplication} = \sum_{m=1}^{M} N_{m-1} \times N_m$$

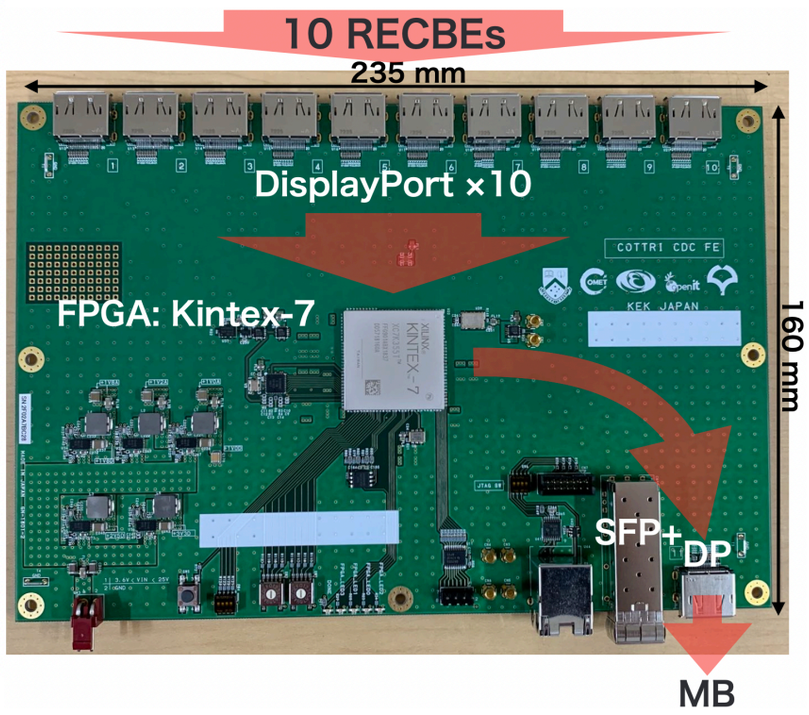
$\propto$DSPs

ハードウェア制約

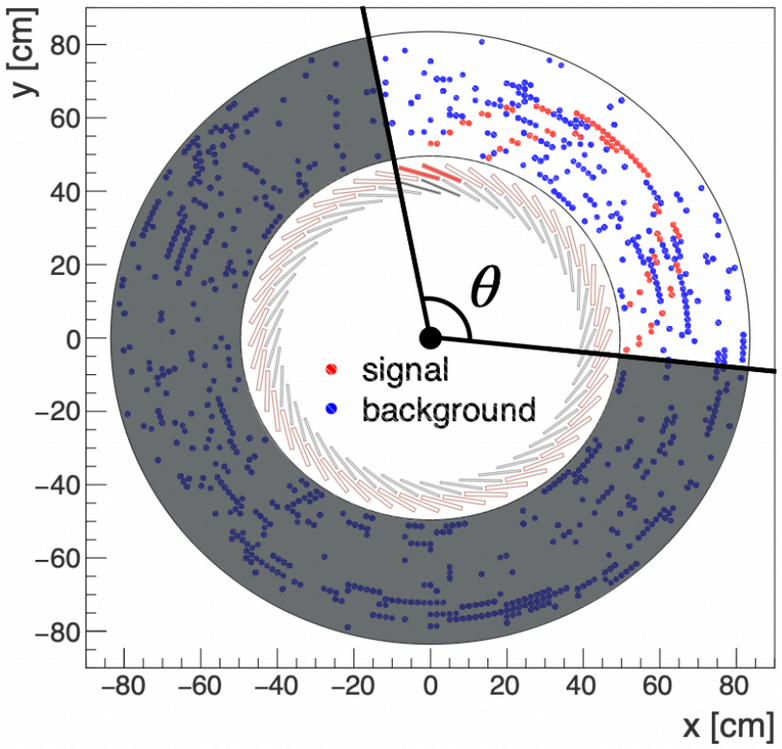
CDC 48 ch



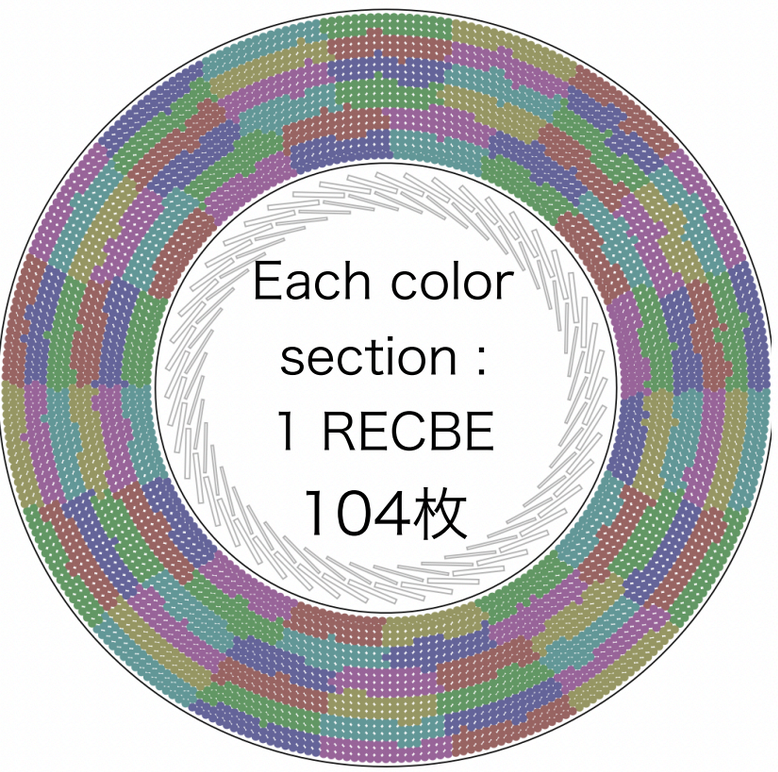
10 RECBEs



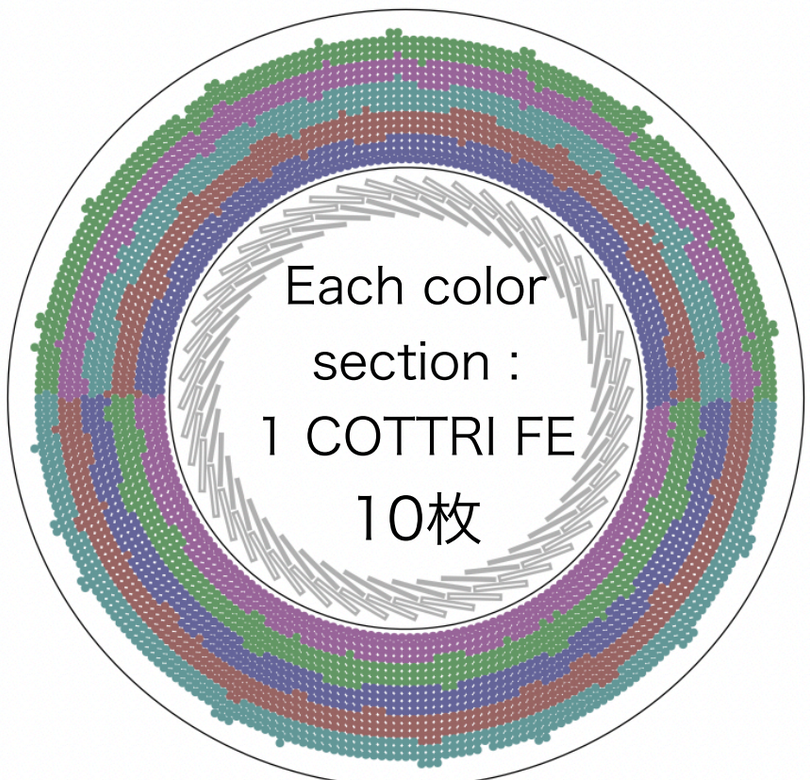
信号電子が軌跡を残すのは
CDCの約1/3領域



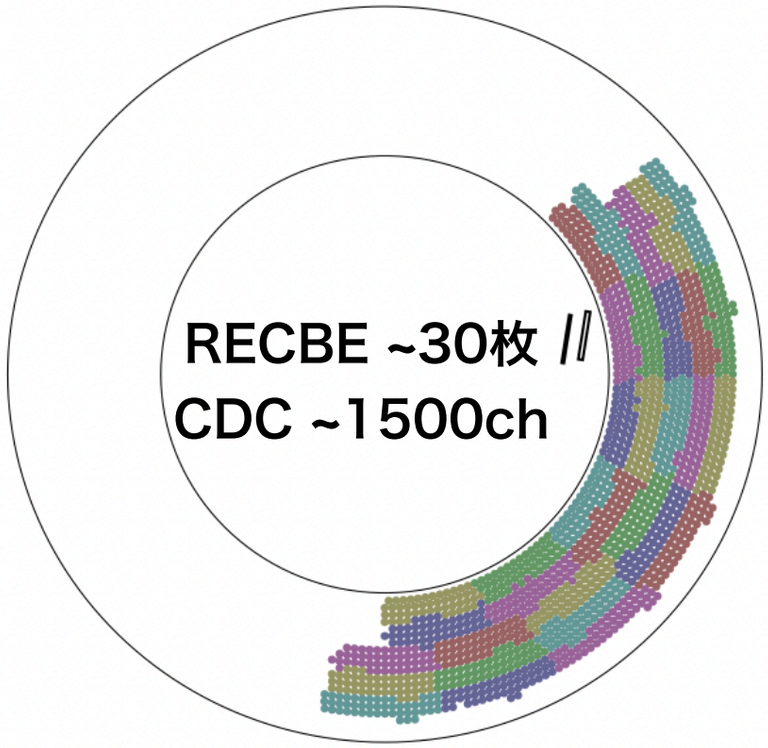
RECBE Configuration



COTTRI FE Configuration



Active sectionの例



Firmware

COTTRI Front-End

Active section
(CDC wire 960 ch)
の1bit score情報を
SiTCPでアドレスに書
き込み

FE-MB間のデータ転送は
10MHz。
960 bit のscoreを
10MHzで転送できないの
で、6bit x 40 に圧縮

Score receiver
1bit x 960chのscore情報

Score sum
1bitのscore情報を24個足して6bit

Aurora 8B/10B
Commu. protocol
Xilinx LogicCORE IP

FPGA
(Kintex-7)

200 MHz

Oscillator
200 MHz

Si5326
Clock Jitter Cleaner
40 MHz to 120 MHz

240 MHz

Clock Module

120 MHz

120 MHz

40 MHz
Through DP

COTTRI Merger-Board

Aurora 8B/10B
Commu. protocol
Xilinx LogicCORE IP

FPGA
(Kintex-7)

120 MHz

120 MHz

Clock Module

240 MHz

QMLP
6 bit x 40 input
16 bit x 2 output

Si5326
Clock Jitter Cleaner
40 MHz to 120 MHz

Oscillator
40 MHz

hls4ml

Firmware

Active section
(CDC wire 960 ch)
の1bit score情報を
SiTCP

Score receiver
1bit x 960chのscore情報

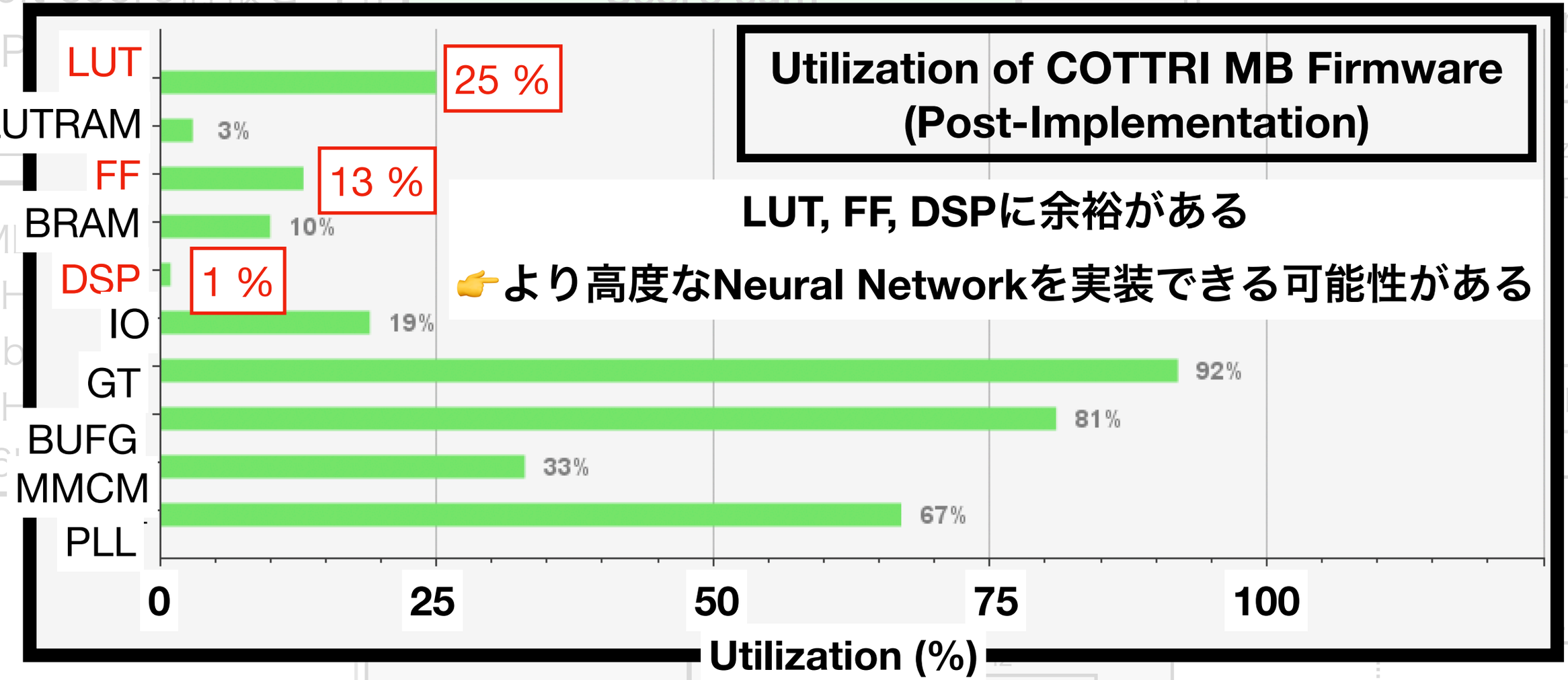
FPGA
(Kintex-7)

200 MHz

Oscillator
200 MHz

Si5326

Score sum



Utilization of COTTRI MB Firmware (Post-Implementation)

LUT, FF, DSPに余裕がある

👉より高度なNeural Networkを実装できる可能性がある

Clock Module

240 MHz

QMLP
6 bit x 40 input
16 bit x 2 output

Oscillator
40 MHz

hls4ml

COTTRI FE to COTTRI MB data format

- Maximum data transfer = 2.4 Gbps/lane x 2lane x 0.8 = 3.84 Gbps
- Data format : 1 header & 10 data packets

1 frame @ 10 MHz

Bit	31	30 29 28 27 26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Header	0	Parity bits	1	Sent number	Board ID
Score	0	Parity bits	0	RECBE 9	
	0	Parity bits	0	RECBE 8	
	0	Parity bits	0	RECBE 7	
	0	Parity bits	0	RECBE 6	
	0	Parity bits	0	RECBE 5	
	0	Parity bits	0	RECBE 4	
	0	Parity bits	0	RECBE 3	
	0	Parity bits	0	RECBE 2	
	0	Parity bits	0	RECBE 1	
	0	Parity bits	0	RECBE 0	

COTTRI FE to COTTRI MB data format

For the preliminary study

1 frame @ 10 MHz

Bit	31	30 29 28 27 26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Header	0	Parity bits	1	Sent number	Board ID
Score	0	Parity bits	0	Input39	Input38	Input37	Input36
	0	Parity bits	0	Input35	Input34	Input33	Input32
	0	Parity bits	0	Input31	Input30	Input29	Input28
	0	Parity bits	0	Input27	Input26	Input25	Input24
	0	Parity bits	0	Input23	Input22	Input21	Input20
	0	Parity bits	0	Input19	Input18	Input17	Input16
	0	Parity bits	0	Input15	Input14	Input13	Input12
	0	Parity bits	0	Input11	Input10	Input9	Input8
	0	Parity bits	0	Input7	Input6	Input5	Input4
	0	Parity bits	0	Input3	Input2	Input1	Input 0

$$precision = \frac{TP}{TP + FP} \qquad recall = \frac{TP}{TP + FN}$$

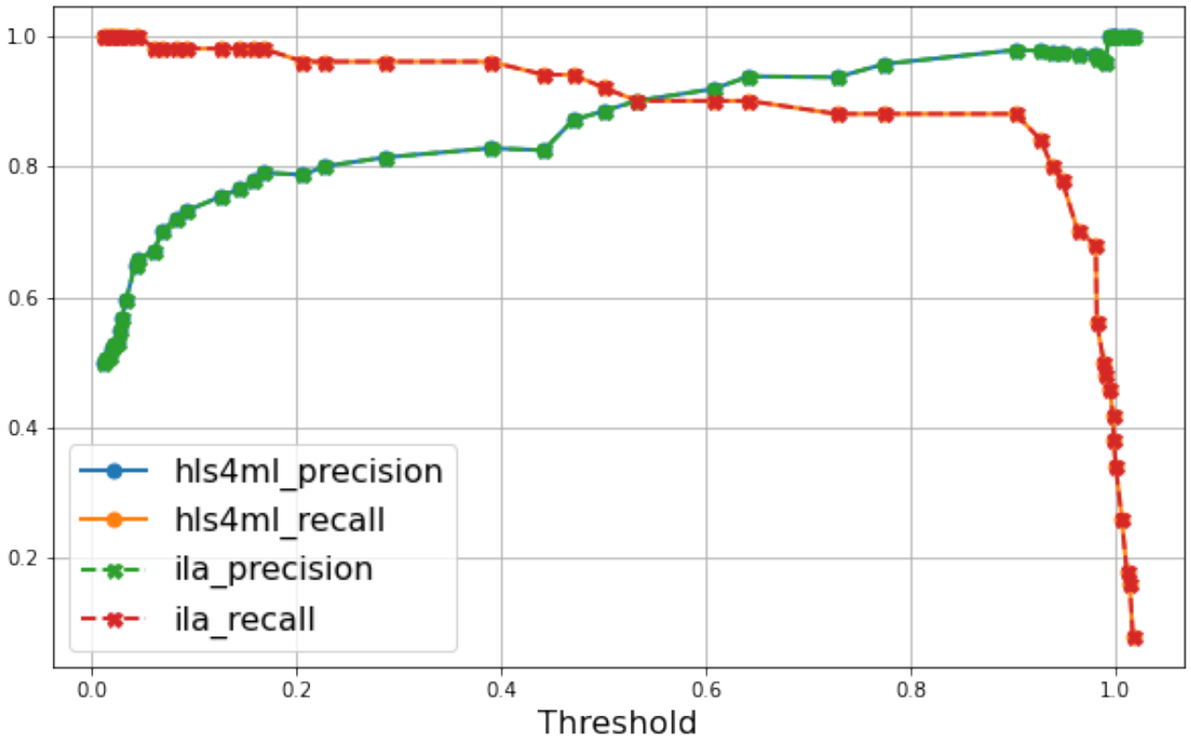
陽性予測の正解率　　正しく分類した陽性の割合

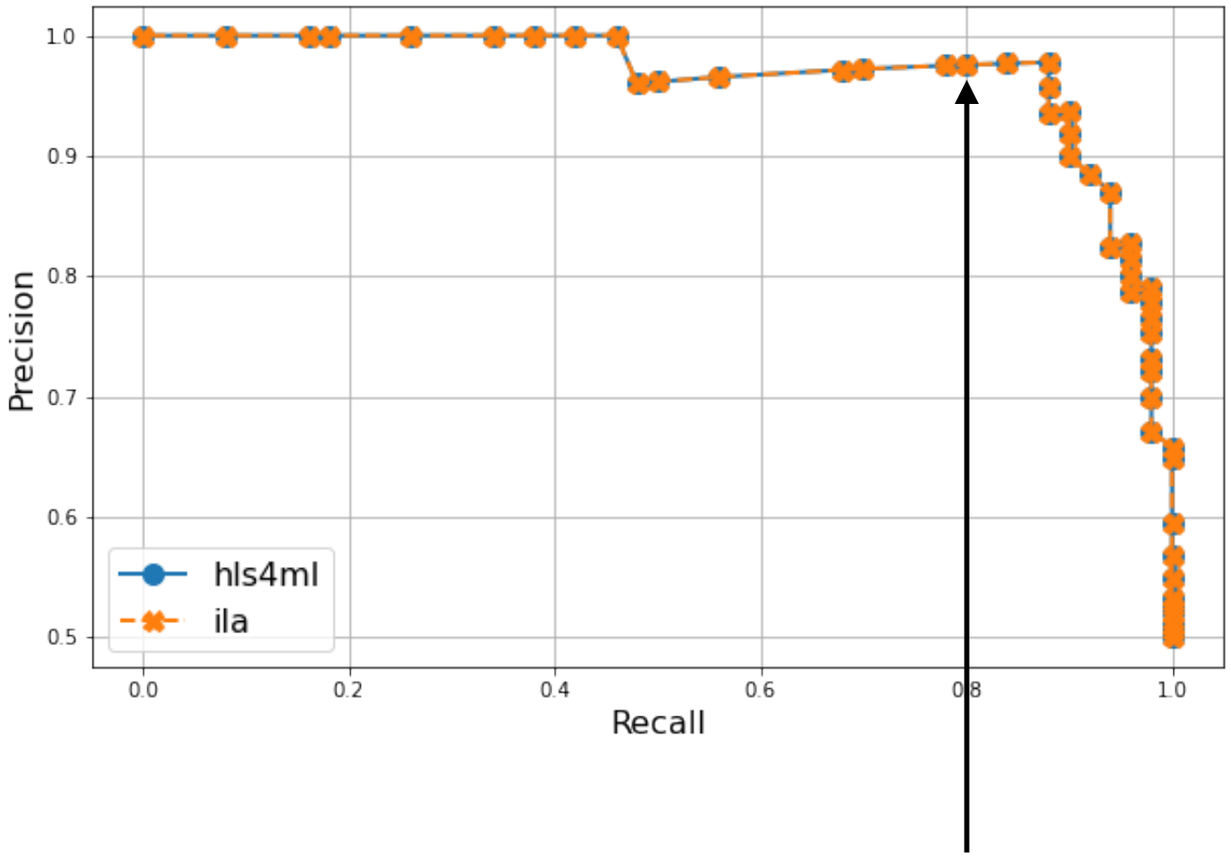
TP : 真陽性の数　Signal eventをsignal eventであると分類した数

TN : 新陰性の数　BG eventをBG eventであると分類した数

FP : 偽陽性の数　BG eventをsignal eventであると分類した数

FN : 偽陰性の数　Signal eventをBG eventであると分類した数





分類器がSignal eventであると予測したとき、その予測が正しいのは98%

全てのSignal eventの80%を検出

$$TPR = \frac{TP}{TP + FN}$$

正しく分類した陽性の割合

$$FPR = \frac{FP}{TN + FP}$$

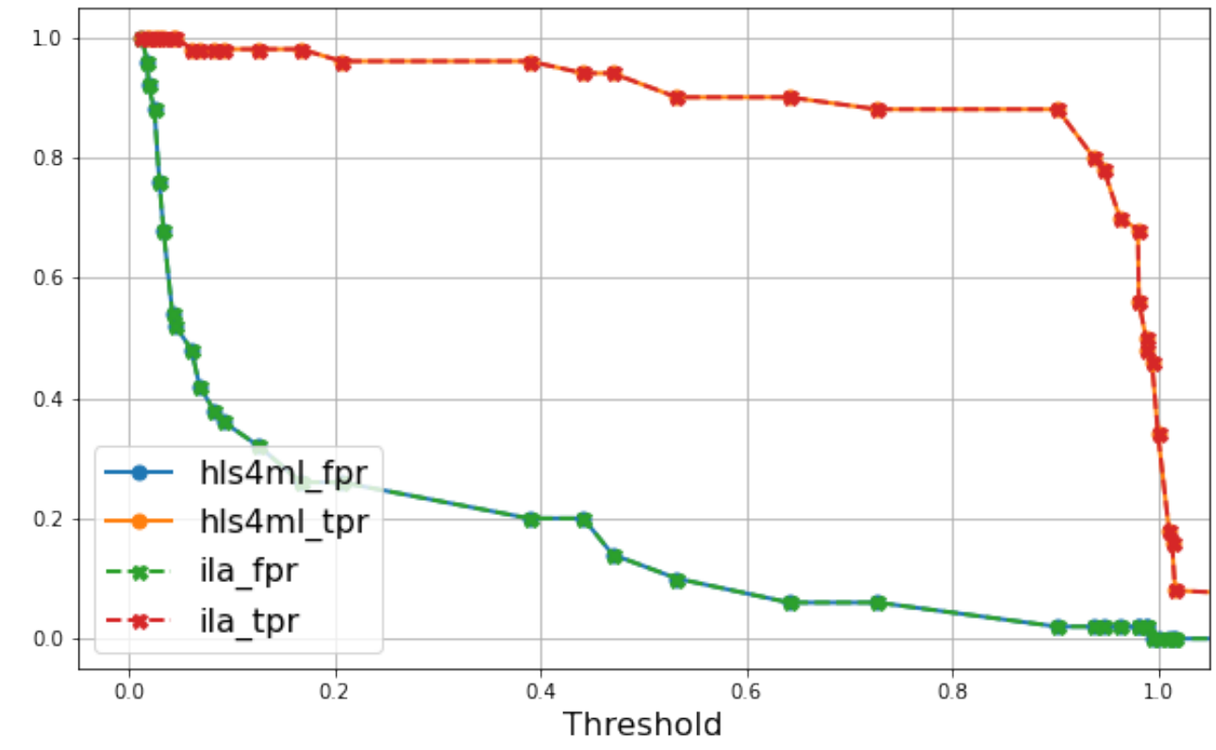
誤って陽性と分類された陰性の割合

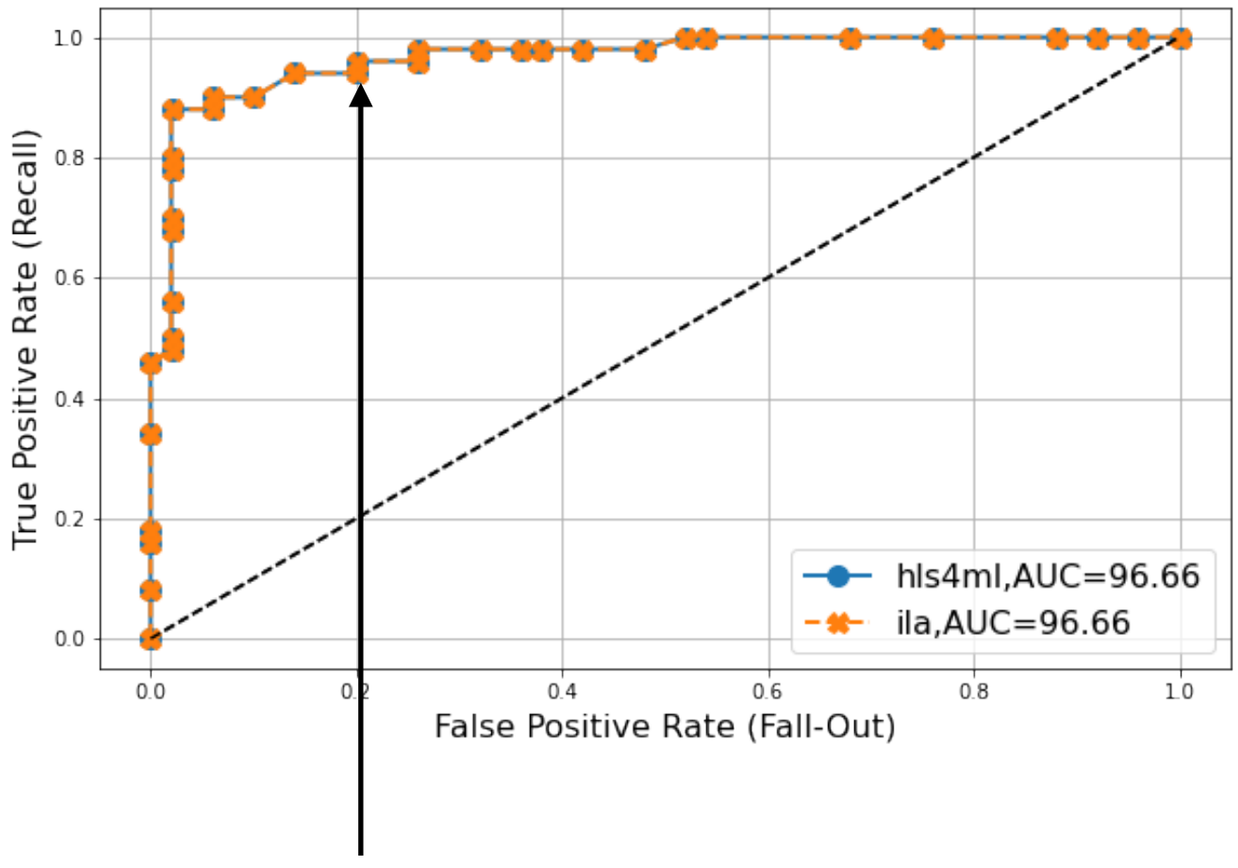
TP : 真陽性の数　Signal eventをsignal eventであると分類した数

TN : 新陰性の数　BG eventをBG eventであると分類した数

FP : 偽陽性の数　BG eventをsignal eventであると分類した数

FN : 偽陰性の数　Signal eventをBG eventであると分類した数





分類器がSignal eventであると予測したとき、その予測が正しいのは98%

全てのBG eventの20%を誤ってSignal eventであると分類